Table 6-6 (cont)

2110 DIAG0	Page Control Register (PCREG) A12U860 (schematic diagram 1): Testing Method: Sets PCREG (bit D7) = 0 and tests for = 0 (stuck at one). Sets PCREG (bit D7) = 1 and tests for = 1 (stuck at zero). If both tests pass, the result flag is set to PASS; otherwise, it is set to FAIL. If test = FAIL then look for failure using the following steps: 1. On the test scope, connect CH 1 to J125 pin 15. Select Slope, + (plus); Trigger Source, CH 1; Trigger Level, 1 V; CH 1 and CH 2 input coupling, DC; CH 1 and CH 2 VOLTS/DIV, 2 V. This step provides a positive, TTL-level trigger strobe (or pulse) for validation of the signal being tested while a test is running. The test scope setup will be used in each of the Registers troubleshooting procedures. Now using CH2 probe: 2. Run test 2110 in CONTINUOUS mode and check for clock activity at U860 pin 11 (clocks on LO-to-HI transition close to the end of the trigger strobe pulse); if not, troubleshoot its clocking circuitry (U884, U862, and U866). 3. Check that U860 pin 19 clocks from LO-to-HI and remains HI after the trigger strobe pulse returns to LO. If not, replace U860. 4. Test for a chip select at U854 pins 1 and 19 (LO enables). If not correct, troubleshoot System Address Decode circuitry (U884, U862, and U866). 5. While selected, check that U854 pin 11 is set to the state of U860 pin 19. If DIAG0 failed and the chip selects to U854 and the signal to U854 pin 11 are ok, then U854 is probably defective.
2120 DCOK U654	Interrupt Register A12U654 (schematic diagram 1) and DCOK logic circuitry A16U395 and associated components (schematic diagram 23): Testing Method: The power supply sends a TTL signal to the interrupt register to inform the System μP of the logic AND of the power supply voltages. DCOK tests INTREG (bit 7). If = 1, the test result = PASS; otherwise, the result = FAIL. Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using CH2 probe: 2. Run test 2120 in CONTINUOUS MODE and check for $\overline{\text{INTREG}}$ chip select on pins 1 and 19 of Interrupt Register U654. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs. 3. While the test is running, test U654 pin 17 for steady-state HI value. If HI and DCOK fails, then replace U654. If LO, then check the power supply voltages and the DCOK AND circuit. If supply voltages are not correct, troubleshoot the low-voltage power supply and regulators; if voltages are correct, troubleshoot A16U395 and associated components (schematic diagram 23).

Table 6-6 (cont)

2130 BUSTAKE	Page Control Register A12U860 (schematic diagram 1), OR-gate A12U332D (schematic diagram 2), and Interrupt Register A12U654: Testing Method: To test for stuck at 1, PCREG U860 is written the pattern x00xxxxx to clear BUS REQUEST and BUSTAKE bits. Then INTREG (bit 6) is tested for = 0, and the PASS/FAIL results are set accordingly. The PCREG is set for a BUSTAKE (x1xxxxxx). This time the INTREG (bit 6) should = 1. The result is set to FAIL if the test fails.
	Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2130 in CONTINUOUS MODE and check for $\overline{\text{INTREG}}$ chip select at U654 pin 1 and 19. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs. 3. Check that BUSTAKE on PCREG U860 pin 16 has LO-to-HI and HI-to-LO transitions on alternate $\overline{\text{PCREG}}$ chip selects. If not, suspect problem with U860. 4. Check INTREG U654 pin 15 for a LO-to-HI transition when BUSTAKE on PCREG U860 pin 16 is set from LO-to-HI; if not, then check U332D (schematic diagram 2) for correct gating.
2140 DIAG1	Processor Miscellaneous Out and Processor Miscellaneous In Registers (A12U750 and A12U854) Diagnostic Bit 1 (schematic diagram 1): Testing Method: This is the first test for the PMISCOUT and PMISCIN registers. The byte to PMISCOUT U760 is set to 00000000 and PMISCIN (bit 4) is tested for = 0. The test result flag is set PASS or FAIL. PMISCOUT is then set to 10000000 and PMISCIN (bit 4) is again tested. If the test fails, the test result is set to FAIL.
	Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2140 in CONTINUOUS MODE and check for chip select at U760 pin 11. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs. 3. Test U760 pin 19 for a LO-to-HI transition between chip selects. If missing, replace U760; if ok, suspect U854.

Table 6-6 (cont)

2150 COMREG	Interrupt Latch (COMREG) A12U550 and Display Status Register (SSREG) A12U542 (schematic diagram 2): Testing Method: A BUSTAKE is executed (previously tested) and the 4Q output of U550 (pin 15) is set LO. SSREG U542 bits 0 and 1 (pins 16 and 18) are then tested to see if they are LO, and the test results are set accordingly. *NOTE* *The inputs of U542 (pins 2 and 4) are wired together.* Pin 15 of U550 is then set HI and SSREG bits 0 and 1 are tested for HI. If the test fails, the test result is set to FAIL.
	Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using CH 2 probe: 2. Run test 2150 in CONTINUOUS mode and check that U550 pin 1 $\overline{\text{(COMREG)}}$ is set LO during the period that the clock line $\overline{\text{(WWR)}}$ to U550 at pin 9 has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 and displaying it at the same time as the clock pulse on U550 pin 9 is acquired. If these signals are not coincident, then troubleshoot the cause and correct the problem. See Figure 6-8 for typical register test waveforms.

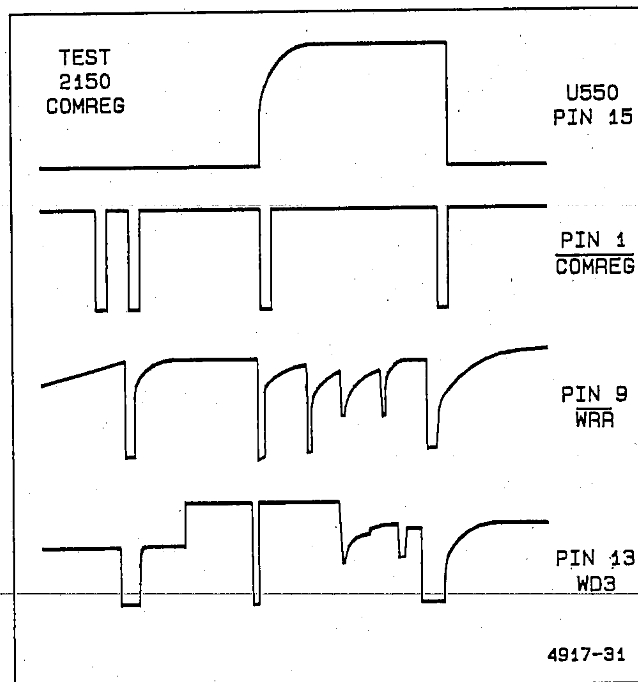

Figure 6-8. Typical Register test waveforms.

Table 6-6 (cont)

3. Check that U550 pin 15 has a LO-to-HI transition after the second clock pulse goes LO-to-HI. If no transition, change U550; if ok, check chip enable of U542 on pin 1 ($\overline{\text{SSREG}}$) to be LO after $\overline{\text{WRR}}$ on U550 pin 9 goes LO-to-HI. If ok, then suspect U550. If the enable is defective, troubleshoot and correct the problem.

2160 WPDN

Waveform μP Done A12U550 (schematic diagram 2):

Testing Method:

A BUSTAKE is executed (previously tested) and pin 10 of Interrupt Latch U550 is set LO. Then pin 14 (bit 2) of PMISCIN register U854 (schematic diagram 1) is tested for a LO, and the test results are set accordingly.

Then pin 10 of U550 is set HI, and U854 pin 14 is tested for a HI. If test fails, the test result is set to FAIL.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH2 probe:

2. Run test 2160 in CONTINUOUS mode and check that U550 pin 1 ($\overline{\text{COMREG}}$) is set LO during the period that the clock to U550 pin 9 ($\overline{\text{WRR}}$) has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 and displaying while acquiring the clock pulse on U550 pin 9. If these signals are not coincident, then troubleshoot the cause.

3. Check that U550 pin 10 has a HI-to-LO transition on the first enable and a LO-to-HI transition after the second clock pulse goes LO-to-HI. If bad, change U550; if good, check chip enable at U854 pins 1 and 19 is LO after U550 pin 10 goes from LO-to-HI. If ok, then suspect U854. If the enable is defective, troubleshoot and correct the problem.

2170 DIAG2

Diagnostic Bit 2 Word Trigger Register A12U754 (diagram 20):

Testing Method

WDREG U754 pin 19 (DIAG2) is set to 0xxxxxxx and PMISCIN A12U854 pin 5 (bit D6) (schematic diagram 1) is tested for 0. The test result is to PASS or FAIL accordingly.

WDREG U754 pin 19 (DIAG2) is then set to 1xxxxxxx and PMISCIN U854 pin 5 (bit D6) is tested for 1. If the test fails, the test result is set to FAIL.

WDREG also drives the GPIB LEDS on the front panel. Bit patterns xxxxx000 to xxxxx111 are sent in a binary sequence with a 50 ms delay between patterns. The register is then reset to entry values.

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Table 6-6 (cont)

	Now using CH2 probe: 2. Check that U754 pin 1 $\overline{\text{RESET}}$ is HI. 3. Run test 2170 in CONTINUOUS mode and check the clock line to A12U754 at pin 11 for LO-to-HI transitions. Since this is the register that provides the strobe to WORD TRIG, there should be four clock pulses, one at each end of the trigger strobe and two under it. If not, troubleshoot the clock source to isolate the problem. 4. Test that U754 pin 19 has a LO-to-HI transition on the third strobe. If there is no LO-to-HI transition, replace U754. If there is, then test A12U854 pin 15 for the same signal as at U759 pin 19. If present, replace U854; if not, find the open.
2180 FLD2	Video Option Mode Register A12U750 (schematic diagram 20): Testing Method: TVREG U750 is set = 00000000 and PMISCIN A12U750 pin 3 (schematic diagram 1) is tested for 0. The test result is set accordingly. TVREG U750 pin 2 (bit D0) is then set to 1 and PMISCIN (bit D7) is tested. If the test fails, the test result is set to FAIL. Troubleshooting Procedure: If test = FAIL then look for failure using the following steps: 1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 2. Run test 2180 in CONTINUOUS mode and check the clock line to A12U750 $\overline{\text{TVREG}}$, pin 11 (schematic diagram 20) for LO-to-HI transitions. There should be two clock pulses under the trigger strobe. If not, troubleshoot the clock source back through Decoder A12U884 (schematic diagram 1) to isolate the problem. 3. Test that U750 pin 2 (FLD2) has a LO-to-HI transition on the second strobe. If there is no LO-to-HI transition, replace U750. If there is, then test U854 pin 17 (schematic diagram 1) for the same signal as at U750 pin 2. If present, replace U854; if not, find the open.
2190 MWPDN	Miscellaneous Register A12U760 (schematic diagram 1): Testing Method: A BUSTAKE is executed (previously tested), Interrupt Latch bit D2 is set true (WPDN) and PMISCOUT Register U760 pin 2 (the mask for WPDN), is set to 0. INTREG U654 pin 18 (bit D0) is tested for 0 and the test result is set accordingly. PMISCOUT U760 pin 2 (bit D0) is set to 1 which should unmask the WPDN that is already set true. INTREG (bit 0) is tested for 1. If test fails, the test result is set to FAIL.

Table 6-6 (cont)

Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

2. Run test 2190 in CONTINUOUS mode and check that A12U550 pin 1 $\overline{\text{COMREG}}$ (schematic diagram 2) is set LO during the period that the clock line U550 pin 9 has a LO-to-HI transition. This may be done by saving the $\overline{\text{COMREG}}$ signal in REF1 (if using a 2440 as the test scope) and displaying it while acquiring the clock pulse on U550 pin 9. If these signals are not coincident, then troubleshoot the cause.

3. Check that U550 pin 2 has a LO-to-HI transition on the second clock pulse. If bad, change U550. If ok, store in REF1 and display it while testing output of A12U880 pin 6 (schematic diagram 1). If ok then replace U654; if not, check the inputs to U880 on pins 4 and 5, and if those are ok, replace U880.

2200
TB-DSP

Display Control Registers (schematic diagram 17):

Testing Method:

Running the test from this level will test all the Display Control registers. These tests will utilize four bit patterns to detect faults. If marked FAIL at this level, go to the lower levels in the menu to test for the failed register. The four bit patterns sent in each of the register tests are as follows:

Test 1—10100101 is sent to the input latch and read back via the output buffer. Test result is set to fail if not a match.

Test 2—01001011 is sent and read back. Test result is set to fail if not a match.

Test 3—10010110 is sent read back. Test result is set to fail if not a match.

Test 4—00101101 is sent and read back. Test result is set to fail if not a match.

NOTE

DISCON (bit 0) will not change, as it has the main board diagnostics as its input.

2210
MISC

Misc Registers A11U532 and A11U540 (schematic diagram 17):

Testing Method:

The MISC register is two components; latch U532 and read-back buffer U540. The test result is set to PASS and the test is done; any failure sets it to FAIL.

If run from this level, all four tests are selected in turn. One may execute any single test by selecting 2211 to 2214. The test involves writing four unique patterns (see test 2200) to U532 and reading them back from U540. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Table 6-6 (cont)

Troubleshooting Procedure:

If test = FAIL for all tests, then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

2. Run test 2210 in CONTINUOUS Mode and check U532 pin 1 for $\overline{MISC}$ to be LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuitry (U550 and U450D) for proper operation.

3. Check U532 pin 19 for clock pulse activity $\overline{WR}$ strobe from System μP).

4. If 1 and 2 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc.

NOTE

Must select test mode of RUN ONCE for stability.

If ok, repeat steps 2 and 3 for U540, and replace U540 if steps 2 and 3 pass.

2220 MODECON

Mode Control Register A11U541 and A11U542 (schematic diagram 17):

Testing Method:

The MODECON register is two components, latch U541 and read-back buffer U542. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn. One may execute any one test by selecting 2221 to 2224. The test involves writing four unique patterns (see test 2200) to U541 and reading them back from U542. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Troubleshooting Procedure:

If test = FAIL for all test then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

2. Check U541 pin 1 for PWRUP = HI; if not, troubleshoot Power Up circuitry (schematic diagram 23).

3. Run test 2220 in CONTINUOUS mode and check U541 pin 11 for clock pulse $\overline{MODECON}$ activity.

NOTE

First clock pulse is the write to U541, the second is the read from U542.

4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc. If ok, replace U542.

Table 6-6 (cont)

2230 DISCON

Display Control Register A11U530 and A11U531 (schematic diagram 17):

Testing Method:

The DISCON (display control) register is two components, latch U530 and read-back buffer U531. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2231 to 2234. The test involves writing four unique patterns (see test 2200) to U530 and reading them back from U531. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

NOTE

The readback bit (bit 0) is the main board diagnostic bit and will not be tested.

Troubleshooting Procedure:

If test = FAIL for all test then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Using the CH 2 probe:

2. Run test 2230 in CONTINUOUS mode and check U530 pin 1 for $\overline{DISCON}$ = LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuit (U550 and U450D) for proper operation.
3. Check U530 pin 11 for clock pulse activity $\overline{WR}$ strobe from System μP).
4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin = 1, D6 pin = 0, etc. If ok, replace U531.

2300 TB-DSP

Display Memory Bus Registers:

Running this test will test all the Display bus registers. There are seven tests in this section. The first two write a pattern to one register and read back from another as in the previous section.

The next three tests deal with the "Q" bus of the display state machine and require strobing of data and shifting of bits for readout.

The remaining two tests use initialized data in U441 and U440 (display and readout memory will be written with our standard four patterns in the first four bites of each memory).

If marked FAIL in the Extended Diagnostic menu, go to the next lower level of diagnostics and run those tests to determine the problem register.

Table 6-6 (cont)

2310 VCURS

Volts Cursors Register A11U241 (schematic diagram 16) Testing Method:

The Volts Cursors Register test checks two components; latch U241 readback is via Diagnostic Buffer U141. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2311 to 2314. The test involves writing four unique patterns (see test 2200) to U241 and reading them back from U141. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Troubleshooting Procedure:

If test = FAIL for all tests then look for failure using the following steps:

1. Check U241 pin 1 to be LO ($\overline{\text{VCURSEN}}$).
2. Check $\overline{\text{VCURS}}$ clock to U241 at pin 11 for activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U241.
4. Check U141 pins 1 and 19 for the $\overline{\text{YDIAG}}$ pulse after the clock pulse to U241. If ok, replace U141. If not present, replace U550 (schematic diagram 17).

2320 TCURS

Time Cursor Register A11U441 (schematic diagram 16):

Testing Method:

The TCURS test checks two ICs; U441 is a latch and the read back is Diagnostic Buffer U243. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2321 to 2324. The test involves writing four unique patterns (see test 2200) to U441 and reading them back from U243. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

Troubleshooting Procedure:

If test = FAIL for all test then look for failure using the following steps:

1. Check U441 pin 1 to be LO ($\overline{\text{TCURSEN}}$).
2. Check U441 pin 11 ($\overline{\text{TCURS}}$) for clock activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U441.
4. Check U243 pins 1 and 19 for the $\overline{\text{XDIAG}}$ pulse after clock pulse to U441. If ok, replace U243; if not present, replace U550 (schematic diagram 17).

Table 6-6 (cont)

2330
U130

Ramp Buffer A11U130 (schematic diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2331 to 2334.

This test requires the display state machine to be operative. There is no "good" way to ensure that it is functional, and there have been no previous tests to help to find that out. Therefore, if this test fails, it could be for several reasons other than U130. If the power-on Self Test starts to run but halts at test level 3000 or test level 6000 (as indicated by the lighted Trigger LEDs), the problem may be in the Display State Machine circuit (schematic diagram 17) or the DISDN signal path to the System µP Interrupt circuit. Use the Display Troubleshooting Chart to troubleshoot the Display State Machine and check that the DISDN signal at U414 pin 5 is correct.

Initialization:

DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENV mode).

MODECON = 00001000. Significant bit is b3 (U140 lower half).

MISC = 00100000. Significant bit is b5 (ZAXIS OFF).

The test result = PASS.

The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe (data loaded to U222 is fixed). Their outputs are selected by U221, U212, U210 holding U414A in the reset mode and not PRESTART. Since the $\overline{\text{STOPDIS}}$ line is LO, the display counters are selected as the source to the Q bus (U210, U212, U221). The inputs to U130 are the bits Q1..Q5 where Q1..Q3 = 0. and Q4, Q5 are the b0, b1 data of pattern. To read back properly, shift the pattern left 3 bits and use only the lower 5 bits of XDIAG (U243).

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Troubleshooting Procedure:

NOTE

Q0 through Q3 = 0. Q4 through Q11 map to D0 through D7; i.e., Q4 = d3. By knowing which test FAILs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort and they must be examined. If all four tests FAIL, then the problem can be in several locations.

Table 6-6 (cont)

1. $\overline{\text{LDCOUNT}}$ might not be strobing the data into Display Counters U220 and/or U211 (schematic diagram 17).
2. U414A may not be resetting, or U323 pin 3 might be HI due to a failure.
3. Address Multiplexers U221, U212, and U210 may not be operating properly.
4. Ramp Buffer U130 (schematic diagram 16) may be defective.

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2230 in CONTINUOUS mode and verify the $\overline{\text{LDCOUNT}}$ strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after $\overline{\text{LDCOUNT}}$ strobe, that the outputs of U222, U220, and U211 are stable and of the correct level for the test selected.
3. Verify that U323 pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text{LDCOUNT}}$ strobe to the previous bus.
5. Verify the chip enable to U130 pins 1 and 15 is LO. If ok to here, replace U130.

2340
U140

Readout Buffer U140 (diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2341 to 2344.

This test requires the display state machine to be operative. There is no "good" way to insure that it is functional and there have been no previous tests. Therefore, if this test fails, it could be for several reasons other than U140.

Initialization:

DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENVELOPE mode).

MODECON = 00001000. Significant bit is b3 (U140 lower half).

MISC = 00100000. Significant bit is b5 (ZAXIS OFF).

The test result = PASS.

The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U140 (lower half) are the bits Q6 through Q8 where Q1 through Q3 = 0. Q4 and Q5 are the b0 and b1 data of the pattern. To read back properly, one shifts the pattern left 3 bits and use bits 4, 5, and 6 of XDIAG (U243); the test result is set to FAIL if the test fails.

Table 6-6 (cont)

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Then MODECON is set to 00010000 to select the top half of U140 and the pattern is shifted left 2 bits. YDIAG (U141) bits 4, 5, 6, and 7 are tested, and the test result is set to FAIL if the test fails.

Test 1. 10100101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

NOTE

Q0 through Q4 = 0. Q4 through Q11 map to D0 to D7. i.e., Q7 = D3. By knowing which test FAILs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort, and the busses must be examined. If all four tests FAIL, then the problem can be in several locations.

1. $\overline{\text{LDCOUNT}}$ might not be strobing the data into U220 and/or U211 (Display Counters, schematic diagram 17).
2. Flip-flop U414A may not be resetting, or OR-gate U323 pin 3 might be HI due to a failure.
3. The busses into or out of Address Multiplexers U221, U212, U210 may not be operating properly.
4. Readout Buffer U140 may be defective.

Troubleshooting Procedure:

Set up the 2430 test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2340 and verify the $\overline{\text{LDCOUNT}}$ strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after $\overline{\text{LDCOUNT}}$ strobe, that the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected.

Table 6-6 (cont)

	3. Verify that U323 pin 3 is LO. 4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text{LDCOUNT}}$ strobe to the previous bus. 5a. Verify the $\overline{\text{RO}}$ chip enable to U140 pin 1 is HI for about half of the Trigger strobe positive period, and then that it goes LO and stays LO for the remaining time. This LO selects inputs Q6 through Q9 of U140. 5b. Verify the $\overline{\text{COUNTEN}}$ chip enable to U140 pin 19 has a HI-to-LO transition; then, before the time that U140 pin 1 goes LO, U140 pin 19 goes HI. While U140 pin 19 is LO, inputs Q6, Q7, Q8 are selected. If ok to here, replace U140.
2350 U240	Readout Buffer U240 (diagram 16): Testing Method: If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2351 to 2354. This test requires the display state machine to be operative. There is no "good" way to insure that it is functional, and there have been no previous tests to help find that out. Therefore, if this test fails, it could be for several reasons other than U240. Initialization: DISCON = 01100000. Significant bits are b2, b5, b6, and b7 ($\overline{\text{STOPDIS}}$, enable "Q" bus, not ENV mode). MODECON = 00010000. Significant bit is b3 (U240). MISC = 00100000. Significant bit is b5 (ZAXIS OFF). The test result = PASS. The test is to load a pattern into the display counters, U220 and U211, with the $\overline{\text{LDCOUNT}}$ strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U240 are the bits Q0 through Q5 where Q0 through Q3 = 0. Q4 and Q5 are the b0, b1 data of pattern. To read back properly, one shifts the pattern left 6 bits and uses bits 6 and 7 of XDIAG (U243); the test result is set to FAIL if the test fails. Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5. Test 4. 00101101 is loaded and read back via U243. Test result is set to FAIL if not a match on bits 0 through 5.

Table 6-6 (cont)

	NOTE *Q0 through Q3 = 0, and Q4 through Q11 map to D0 to D7. i.e., Q7 = D3. By knowing which test FAILs and the bit pattern, one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).* If 2 or 3 tests fail, then there is a bus problem of some sort that must be examined. If all four tests FAIL, then the problem can be in several locations. 1. $\overline{LDCOUNT}$ might not be strobing the data into U220 and/or U211. 2. Flip-flop U414A may not be resetting, or U323 pin 3 might be HI due to a failure. 3. Address Multiplexers U221, U212, and U210 may not be operating properly. 4. Readout Buffer U240 may be defective.
	Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. Now using the CH 2 probe: 1. Run test 2350 in CONTINUOUS mode and verify the $\overline{LDCOUNT}$ strobe pulse at pin 11 of U222, U220, and U211. 2. Verify that after $\overline{LDCOUNT}$ strobe, the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected. 3. Verify that U323A pin 3 is LO. 4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{LDCOUNT}$ strobe to the previous bus. 5. Verify the $\overline{RO}$ chip enable to U240 pins 1 and 15 is LO. If ok to here, replace U240.
2360 U322	Vertical Buffer U322 (diagram 16): Testing Method: If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2361 to 2364. The contents of the first four bytes of U322 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U322 is decoded by reading address 2000h. Set test result = PASS. If contents of 2000h not equal to 10100101, then test result = FAIL. If contents of 2001h not equal to 01001011, then test result = FAIL. If contents of 2002h not equal to 10010110, then test result = FAIL. If contents of 2003h not equal to 00101101, then test result = FAIL.

Table 6-6 (cont)

Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Using the CH 2 probe:

1. Run test 2360 in CONTINUOUS mode and check U322 pin 19 for a negative strobe $\overline{YSEL}$ at 10 μs from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.

2. Check for activity on the $\overline{WRD}$ signal line of U322 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).

3. Check that the data pattern for the test is correct at the input and output pins of U322. The data is stable during the $\overline{YSEL}$ strobe on pin 19, and the data bit level must be read in coincidence with it as other activity is also taking place on the WD bus. A Word Recognizer probe would be useful to make these checks, but it is not necessary.

4. If the input and output data patterns of U322 do not match, replace U322. If they match each other, but are not correct, suspect a problem with Vertical RAM U431. Run test 2361 through test 2364 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests.

5. Check pin 20 $\overline{(DEY)}$ and pin 18 $\overline{(CSY)}$ of U431 for a negative strobe coincident with the $\overline{YSEL}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.

6. Check that pin 21 of U431 $\overline{(WE)}$ is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the $\overline{WE}$ signal is not correct, troubleshoot U422 and the input signals to it.

7. Replace U431.

2370
U314

Horizontal Buffer (diagram 16):

Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2371 to 2374. The contents of the first four bytes of U314 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U314 is decoded by reading address 2800h.

Set test result = PASS.

If contents of 2800h not equal to 10100101, then test result = FAIL.

If contents of 2801h not equal to 01001011, then test result = FAIL.

If contents of 2802h not equal to 10010110, then test result = FAIL.

If contents of 2803h not equal to 00101101, then test result = FAIL.

Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Table 6-6 (cont)

Using the CH 2 probe:

1. Run test 2370 in CONTINUOUS mode and check U314 pin 19 for a negative strobe $\overline{\text{XSEL}}$ at 10 μs from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.

2. Check for activity on the $\overline{\text{WRD}}$ signal line of U314 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).

3. Check that the data pattern for the test is correct at the input and output pins of U314. The data is stable during the $\overline{\text{XSEL}}$ strobe on pin 19, and the data bit level must be read in coincidence with it, as other activity is also taking place on the WD bus.

4. If the input and output data patterns of U314 do not match, replace U314. If they match each other, but are not correct, suspect a problem with Horizontal RAM U431. Run test 2371 through test 2374 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests. A Word Recognizer probe would be useful for making these checks but is not necessary.

5. Check pin 20 ($\overline{\text{DEX}}$) and pin 18 ($\overline{\text{CSX}}$) of U440 for a negative strobe coincident with the $\overline{\text{XSEL}}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.

6. Check that pin 21 of U440 ($\overline{\text{WE}}$) is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the $\overline{\text{WE}}$ signal is not correct, troubleshoot U422 and the input signals to it.

7. Replace U440.

2400 TB-DSP

Running the test at this level will execute the Time Base Controller (U670) tests for Short-Pipe (SISO) and FISO modes.

The test causes Time Base Controller U670 to simulate all the necessary states to get an acquisition in Short-Pipe and FISO modes.

2410 U670 FISO

Time Base Controller A11U670 (schematic diagram 8):

Running the test executes the Time Base Controller in FISO mode.

Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2410 in the CONTINUOUS mode. Set the Sec/Div setting of the test scope to 1 μs and connect the CH 2 probe to pin 19 of bidirectional buffer U641 ($\overline{\text{TBSEL}}$); save CH 2 into REF1 and Display REF1.

2. Position CH 2 down to allow room and connect the CH 2 probe to U641 pin 1; save CH 2 into REF2 and Display REF2. The LO $\overline{\text{TBSEL}}$ pulse should be coincident to a HI $\overline{\text{RD}}$ pulse; if not, then troubleshoot the $\overline{\text{TBSEL}}$ or the $\overline{\text{RD}}$ signal line.

Table 6-6 (cont)

3. Position CH 2 down to allow room to display the signal and probe U641 pin 11 through 18. While the REF1 signal $\overline{\text{TBSEL}}$ is LO and REF2 signal $\overline{\text{RD}}$ is HI, compare the results to 01100101 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641.

4. Test the output of U670 pin 26 for a square wave with a period of about 200 μs. If not correct, replace U670.

5. If present, test for the square wave at U680 pin 16; replace U680 if TIMER signal is missing.

6. If all checks were ok, suspect A12U542 (schematic diagram 2).

2420
U670 SISO

Time Base Controller A11U670 (schematic diagram 8):

Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure and run test 2420 in the CONTINUOUS mode on the scope under test.

Now using the CH 2 probe:

1. Position the trigger strobe (CH1) near the top of the crt and connect the CH 2 probe to pin 19, $\overline{\text{TBSEL}}$, of U641. Adjust the Sec/Div setting of the test scope to 1 μs. Verify that there is a negative $\overline{\text{TBSEL}}$ pulse during the positive trigger strobe. Save the CH 2 waveform in REF1 and display REF1.

2. Position the CH 2 display down to allow room and connect the CH 2 probe to U641 pin 1. Save CH 2 into REF2 and display REF2. The $\overline{\text{TBSEL}}$ pulse should be coincident to a HI $\overline{\text{RD}}$ pulse; if not, then troubleshoot the chip select or $\overline{\text{RD}}$ signal line.

3. Position the CH 2 display down to allow room and probe U641 pin 11 through 18 while REF1 signal is LO and REF2 signal is HI. Compare the results to 01000000 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641.

4. Test the output of U670 at pin 26 for a square wave signal (TIMER) with a period of about 200 μs; if not present, replace U670.

5. If present, test for the square wave at U680 pin 16 and replace U680 if missing.

6. If all checks were ok, suspect A12U542 (schematic diagram 2).

2500
MAIN

The MAIN board has five shift-register tests. These are in two groups. The first group includes Gate Array U270, Peak-Detector U530, Attenuators U511 and U221 (acting as one 16-bit register), Trig U140. The second group has the System-DAC U850 and U851 (acting as one 16-bit register).

From this level, the initialization and all five tests are selected in turn. An individual test may be run by selecting test numbers 2510 to 2560.

There is one diagnostic bit for readout off the main board and that is the logic-AND of the MSB of all the shift registers. The shift registers are preset to 10100101, or 1010010110100101 and the diagnostic bit is tested to see if a "1" is being read out for the MSB. If the diagnostic bit is not = 1, then either one of the registers is not loading or the diagnostic bit is stuck. In any event, no further meaningful data is possible, so the test stops. If initialization is successful, each bit is shifted out, register by register, and compared against what it should be by shifting the initial pattern and comparing the MSB. After any register is tested, it is reinitialized so the next register may be tested. Discon (input = U531 pin 18, output = U531 pin 17) is the diagnostic bit from the main board.

Table 6-6 (cont)

Test	Description
2510 INIT SHIFT REGS	Acquisition Control Shift Registers A10U270 (Gate Array), A10U530 (Peak Detector), A10U140 (Trig Control), DAC Input Shift Register A10U850/U851 (schematic diagram 5), and Attenuator Shift Register A10U221/U511 (schematic diagram 9): Testing Method: For this test to pass, the MSB of the five output registers above must be high. If one of the registers didn't have the correct pattern strobed in, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. Run test 2510 in CONTINUOUS mode. Using the CH 2 probe: 1. Check A10U380 pin 3 (schematic diagram 5) for a HI level during the HI period of the trigger strobe. If ok, then check for the same signal at A11U531 pin 18 (schematic diagram 17). If correct and test is failing, replace U531 and run SELF DIAG. 2. Check U380 pins 1 and 2. If both are HI during the trigger strobe HI and pin 3 does not follow, then replace U380. If neither pin 1 nor 2 is HI, then suspect DAC Select Multiplexer U272 or its input gating. 3. If U380 pin 2 is LO, then run test 2560 and troubleshoot using the procedure given for that number. 4. If U380A pin 1 is LO, then find which cathode of the input diodes (CR185, CR186, CR286, or CR287) is LO. Run the test number for the suspected Shift Register and check the inputs (clocks, data, and power) to it (look at the information given with the test number for the troubleshooting procedure for each Shift Register). If they are all ok, replace the suspected Shift Register; if not, troubleshoot the bad input.
2520 ATTEN	Attenuator Shift Registers A10U221/A10U511 (schematic diagram 9): Testing Method: For this test, the MSB of A10U511 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. NOTE *For the following, set the Trigger Position of the test 2430A to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2520 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U511 pin 9 and U221 pin 9 for +5 V (registers not held reset). If not +5 V, then repair. 2. Check Shift Register U221 at pin 8 for activity (ATT SR CLOCK line). If clock is missing, troubleshoot Control Register Clock Decoder A10U271 (diagram 5).

Table 6-6 (cont)

	3. Check U221 pins 1 and 2 for activity (ACD line is the data input). If ACD missing, troubleshoot the signal path to and gating on the inputs of DAC Multiplexer Select register U272 (diagram 5). 4. Check U221 pin 13 for activity; replace U221 if inactive. 5. If checks good to this point and the test still fails, replace U511.
2530 PEAK DETECTOR	Acquisition Control Register A10U530 (schematic diagram 5): Testing Method: For this test, the MSB of A10U530 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. NOTE *For the following, set the Trigger Position of the test scope to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2530 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U530 pin 9 for a HI level. If LO, then check R531 and source of +5 V. 2. Check U530 pin 8 for activity (PD SR CLK signal line); if inactive, repair. 3. Check U530 pins 1 and 2 for activity (ACD line is the data input). Repair if inactive. 4. If all inputs are good, replace U530.
2540 GATE ARRAY	Acquisition Control Register A10U270 (schematic diagram 5): Testing Method: For this test, the MSB of U270 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2100 troubleshooting procedure. NOTE *For the following, set the Trigger Position of the test 2430A to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2540 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U270 pin 9 for a HI level. If not +5 V, check R269 and source of the +5 V. 2. Check U270 pin 8 for activity (GA SR CLK signal line); if inactive, repair. 3. Check U270 pins 1 and 2 for activity (ACD line is the data input). Repair if inactive. 4. If all inputs are good, replace U270.

Table 6-6 (cont)

2550 TRIG	Acquisition Control Register A10U140 (schematic diagram 5): Testing Method: For this test, the MSB of A10U140 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. NOTE *For the following, set the Trigger Position of the test 2440 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2550 in CONTINUOUS mode. Using the CH 2 probe: 1. Check U140 pin 9 for a HI level ($\overline{\text{RESET}}$). If LO, repair. 2. Check U140 pin 8 for activity (TRIG CONT CLK line). If inactive, repair. 3. Check U140 pins 1 and 2 for activity (ACD line is the data input); repair if inactive. 4. If all inputs are good, replace U140.
2560 SYSTEM DAC	DAC Input Shift Registers A10U850/A10U851 (schematic diagram 5): Testing Method: For this test, the MSB of A10U851 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails. Troubleshooting Procedure: Set up the test scope as in Step 1 of the 2110 troubleshooting procedure. NOTE *For the following, set the Trigger Position of the test 2440 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.* Run test 2560 in the CONTINUOUS mode. Using the CH 2 probe: 1. Check U850 pin 9 and U851 pin 9 for HI level. If not +5 V, check R850 and source of the +5 V. 2. Check U850 pin 8 and U851 pin 8 for clock activity. If clocks are inactive, then: a. Check U280B pin 5 to have a LO gate present; replace U272 if pin 5 is stuck either HI or LO. b. Check U280B pin 6 for clocking signals during the HI period of the trigger strobe. c. Replace U280 if not gating correctly; troubleshoot clock signals if not present. 3. Check the data input to U850 at pins 1 and 2. The signal should be a train of pulses during the HI period of the trigger strobe. If the data input signal is not present, test signals around U280D and correct.

Table 6-6 (cont)

4. Check U850 pin 13 that the first 8-bits of the 16-bit pattern comes out as the second is shifted into U850 at pins 1 and 2. (A Sec/Div setting of 0.5 ms on the test scope is good for viewing the data pattern, and the latched data on pin 13 is much easier to view than the input data pulses). If the data is not shifting through U850, then replace U850.

5. If the data is coming through U850, check U851 pins 1 and 2 to verify that it is ok there. Check pin 13 of U851 for a data pattern of 1010010110100101. (Each bit is approximately 0.2 ms wide, so a 0.4 ms wide pulse is two bits.)

6. Replace U851 if not shifting the signal through.

2600
SIDE U761/U762

Holdoff Register A11U762 (schematic diagram 13):

Testing Method:

From this level, all four tests are selected in turn. Individual test may be called by selecting test numbers 2610 to 2640. The test involves writing 4 unique patterns to U762 and reading them back from U761. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test FAILs and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

The HOREG register is two integrated circuits; U762 is a latch and the read back is U761. If all tests pass, the test result is set to PASS; any failure sets it to FAIL.

NOTE

Bit 3 of the test patterns is not allowed to be set LO as it would reset the GPIB chip and we cannot restart it from the diagnostic routines.

Test 1. 10101101 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.

Test 2. 01001011 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.

Test 3. 10011110 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.

Test 4. 00101101 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.

Troubleshooting Procedure:

If the failure occurs for all tests:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using CH2 probe:

1. Check that U762 pin 1 $\overline{\text{HOREG}}$ is LO about 12 μs after the trigger strobe. If $\overline{\text{HOREG}}$ is absent, test the inputs of U781. Replace U781 if the inputs are ok; if not ok, troubleshoot that problem.

2. Check that U762 pin 9 ($\overline{\text{WR}}$ clock) has a LO-to-HI transition during the enable time. (Save enable in REF1 and display it while looking at the clock.) Clock line is the write line; if missing, suspect open run or connection.

3. Check the outputs U762 (pins 15, 12, 10, 7, and 5) for the proper levels for the pattern that is being looped on. Replace U762 if incorrect.

4. Check U761 pin 1 to be enabled after the clock to U762 pin 9. If present, then the problem is possibly U762.

Table 6-6 (cont)

3000
SYS-RAM

All RAM tests are non-destructive. The Display RAM is tested first, and, if found good, the contents of the other RAMs are stored in the Display RAM as they are tested. The contents are returned after the test is complete.

From this level (3000), all eight RAM tests are selected in turn. An individual RAM test may be run by selecting test levels 3100 to 3800.

NOTE

An internal jumper, A13J156, must be removed before test levels 3700 and 3800 may be run. If the jumper is removed and test levels 3700 and 3800 are run, loss of power during while they are running can result in loss of internal calibration constants. In that event, a partial recalibration is required (see information regarding power loss while running SELF CAL under "Diagnostics" in this section). Run these tests only if necessary.

3100 A11U431	**3500 A11U600**
3200 A11U440	**3600 A12U440**
3300 A12U350	**3700 A12U664**
3400 A11U430	**3800 A12U664**

Each RAM test (levels 3100-3800) is comprised of the four following subparts:

A logic one is shifted left through a field of logic zeros while incrementing the address (the "−" TRIGGER SLOPE LED is lit).

A logic one is shifted right through a field of logic zeros while decrementing the address (the "+" TRIGGER SLOPE LED is lit).

A logic zero is shifted left through a field of logic ones while incrementing address (the "−" TRIGGER SLOPE LED is lit).

A logic zero is shifted right through a field of zeroes while decrementing the address (the "+" TRIGGER SLOPE LED is lit).

Running level 3000 causes all four parts of the test to be performed on all 8 RAMs (sublevels 3100-3800), while running an individual sublevel test causes the four-part test to be performed on the corresponding RAM device.

Running a sublevel test from 3×10 to 3×40 (where × = 1-8) runs the part (out of four parts) indicated by the test label (for instance, "3340 1←0S" runs the test that shifts logic 0 left in a field of logic ones for an incrementing address on U350).

3100
A11U431

RAM A11U431 (schematic diagram 16):

Troubleshooting Procedure:

If test = FAIL then look for failure and correct using the following steps:

Using the CH 1 probe:

1. Run test 3110 in CONTINUOUS mode and check for activity on the chip select line to U431 ($\overline{CSY}$, pin 18). If active, trigger the test scope on the signal. If no chip select, work backwards and find problem.

Using the CH 2 probe:

2. Check for activity on the write enable line to U431 ($\overline{WE}$, pin 21) and note that it is LO at the same time as the chip select line. If no signal present, work backwards and find the problem.
3. Check for activity on the output enable line to U431 ($\overline{DEY}$, pin 20). If none, work backwards and find the problem.
4. Check the data I/O pins of U431 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3100 is selected. If no activity when $\overline{DEY}$ (output enable) is LO (pin stuck HI or LO), then suspect U322; otherwise suspect U431.

Table 6-6 (cont)

3200 A11U440	RAM A11U440 (schematic diagram 16): Troubleshooting Procedure: If test = FAIL then look for failure and correct using the following steps: Run test 3210 in CONTINUOUS mode. Using the CH 1 probe: 1. Check for activity on the chip select line U440 ($\overline{CSX}$, pin 18, and trigger the scope on the CH 1 signal. If none, work backwards and find problem. Using the CH 2 probe: 2. Check for activity on the write enable line U440 pin 21, and note that it is LO at the same time as the chip select line. If none, work backwards and find the problem. 3. Check for activity on the output enable line U440 pin 20. If none, work backwards and find the problem. 4. Check the data I/O pins U440 (pin 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3210 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect U314; otherwise suspect U440.
3300 A12U350	RAM A12U350 (schematic diagram 2): Troubleshooting Procedure: If test = FAIL then look for failure and correct, using the following steps: Select test 3310 and RUN CONTINUOUSLY. Using the CH 1 probe: 1. Check for activity on the pin 20 chip select line to U350, and trigger the scope on the signal if active. If no chip select, work backwards through the chip select circuitry and find problem. 2. Check for activity on the write enable line to U350 ($\overline{WRR}$, pin 27) and note that it is LO at the same time as the chip select line. If no activity, work backwards and find the problem. 3. Check for activity on the output enable line to U350 ($\overline{WRD}$, pin 22). If no activity, work backwards and find the problem. 4. Check the data I/O pins U350 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3400 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect buffer U352; otherwise suspect U350.

Table 6-6 (cont)

3400 A11U430	RAM A11U430 (schematic diagram 16): Troubleshooting Procedure: If test = FAIL then look for failure and correct using the following steps: Run test 3410 in CONTINUOUS mode. Using CH 1 probe: 1. Check the write enable to U430 ($\overline{WRA}$, pin 8) for activity and trigger on the signal if active. If no activity, troubleshoot OR-gate U422A and U422C and their input signals. Check that pin 10 is LO; if not, repair. Using the CH 2 probe: 2. Check for activity at the data input to U430 (DI, pin 11) timed with the enable pulse. If no signal, suspect U423A or U422B. 3. If the checks in Steps 1 and 2 are ok, replace U430.
3500 A11U600	ACQUIRE RAM A11U600 (schematic diagram 8): Troubleshooting Procedure: If test = FAIL then look for failure and correct, using the following steps: Run test 3510 in CONTINUOUS mode. 1. Check for LO on chip select line U600 pin 18. Repair if not LO. 2. Check for activity on the write enable line to U600 ($\overline{WE}$, pin 21). If no activity, work backwards and find the problem. 3. Check for activity on the output enable line to U600 ($\overline{OE}$, pin 20). If no activity, work backwards and find the problem. 4. Check the data I/O pins of U600 (pins 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3500 is selected. If no activity (stuck HI or LO) when the output enable is LO, then suspect buffer U610; otherwise suspect U600. 5. Check the address lines (MA0-MAA) for activity. If no activity on any lines, troubleshoot the $\overline{WE}$ and TB2MEM signals to U300, U400, and U410. If an address line is stuck, troubleshoot that problem.
3600 A12U440	CMD/TMP RAM A12U440 (schematic diagram 2): *NOTE* *If tests 3300 through 3600 all fail, the most likely faults are: a stuck data line to A12U352, a bad select signal to A12U352, or Waveform Data Buffer A12U352 itself.*

Table 6-6 (cont)

	Troubleshooting Procedure: If test = FAIL then look for failure and correct, using the following steps: Run test 3610 in the CONTINUOUS mode. Using the CH 1 probe: 1. Check for activity on the chip select line to A12U440 (pin 20), and trigger the scope on the signal if active. If no activity, work backwards through U250C and find the problem. Using the CH 2 probe: 2. Check the data I/O pins of U440 (pins 11, 12, 13, 15, 16, 17, 18, and 19) for activity. If no activity when output enable is LO, then suspect U440; otherwise check U352.
3700 or 3800 A12U664	A12U664 (schematic diagram 2) NOTE *The test of RAM device A12U644 is divided into two test levels, 3700 and 3800. The sections of U644 that may be accessed depends on the condition of the BUSREQ output of A12U860. With BUSREQ set HI, the 8K×8 memory space corresponding to addresses 7000H to 8FFFH is the only space available; with BUSREQ set LO, the 24K×8 memory space corresponding to addresses 0000H to 5FFFH are both available. Level 3700 tests the 7000H to 8FFFH block while level 3800 tests the 0000H-5FFF block resulting in the entire 32K×8 RAM being tested. The Troubleshooting Procedure that follows applies to both test levels.*
	Troubleshooting Procedure: NOTE *If the System Ram data bus, chip selects, or output enable lines are defective, the System µP cannot run the the diagnostics testing. Therefore, if test 3700/3800 fails, the most likely problem is U664. If the diagnostics tests do not run, the Kernel test will have to be used to isolate a system bus or address decoding problem. An NV RAM failure due to stored data being scrambled requires a "COLD START" to reload the NV RAM with correct nominal values. The COLD START should be followed by a SELF CAL and then an EXTENDED CAL of ATTEN, TRIGGERS, and REPET to return it to a completely calibrated state.* If test = FAIL, look for failure and correct using the following steps: Run test 3710 or 3810 in CONTINUOUS mode. Using the CH 1 probe: Check for a LO on pin 20. If it is HI, check back to the source of the problem starting with Q960. Check for a HI on chip select 2 (pin 26). If not HI, check back to the source of the problem start with U424A.

Table 6-6 (cont)

	Using the CH 2 probe: Check for activity on the write enable line pin 27. Check for activity on the output enable line pin 22. Check the data I/O pins (pins 11, 12, 11, 15, 16, 17, 18, 18) for activity. Check the data I/O pins (pins 11, 12, 13, 14, 15, 16, 17, 18,) of U660 for activity. If not active, check its write enable and output enable lines (pins 1, 19).
4000 FPP	Front Panel μP A13U700 (schematic diagram 3): Testing Method: The Front Panel Processor test first sets all test results to NULL. Any failure to complete all the tests will result in a locked front panel. Depending on the nature of the failure, the Trigger LEDS may be latched in the first number of the test level that failed, the failure code may be flashed out on the LEDs (if it is the first failed test), or it may make it through the diagnostic, but with the FPP test marked FAIL. That information will help to isolate which circuitry may be defective and gives the starting point in troubleshooting a failure. It will be necessary to turn off the scope and turn it back on again to repeat the diagnostic testing from the front panel; however, testing may be done using GPIB diagnostic test commands. The Front Panel μP internal diagnostics require that the μP be reset. Therefore, the structure of the FPP tests is such that the processor is initialized when completed. This requires that ALL of the tests be run in order. Therefore, all tests will be run even though it appears that only a sub-test is being executed. Test Steps: 4100 U861 pin 9 should be reset to its LO state via U862B and U862A. 4200 U861 pin 6 should be reset to its HI state via U862C and U862D. 4300 U861 pin 9 (WR TO HOST) should clock pin 9 HI. 4400 U700 (Front Panel μP) checks its internal RAM, ROM, Timer, and A/D. Any failure will set the test result to FAIL. 4500 U861 pin 6 (FPDNRD) should clock pin 6 LO. 4600 U742 and U751. Four bit patterns are written to the FPP and echoed back. If these are not returned properly, the test result = FAIL. Troubleshooting Procedure: Failure of one of the Front-Panel μP tests may be indicated only by flashing out the failed test number on the Trigger LEDs, but if the diagnostic testing can continue past the failure, the Extended Diagnostic menu will be seen with the FPP test marked FAIL. The usual result of a Front Panel μP failure is a locked up front panel (the button and pots will not be functional). To rerun the diagnostic testing from the front panel to check the Trigger LEDs for the failed test number, it is necessary to turn off then turn back on the scope.

Table 6-6 (cont)

Troubleshooting Front-Panel μP A13U700:

1. Check pin 5 for the 4 MHz clock.
2. Check pin 4 for +5 V, pin 1 for ground.
3. Check pins 8, 14, 16, 17, 19, 31, and 32 for +5 V and pins 6, 7, and 20 for ground.
4. Perform the Front Panel μP test if all the checks in steps 1, 2, and 3 were ok. If not, troubleshoot any problem area found by the checks.

Front Panel μP Test:

1. Turn off power and short pins 1 and 2 of J155 together. (The pins must remain shorted together during power-on.) This places the Front-Panel μP in the continuous self-diagnostic mode (Test 4400). Connect a test scope to view the signal present on pin 14 of U700.
2. Turn the power back on and observe the signal at pin 14. See test waveform illustration of Figure 6-9 for correct waveshape and timing.

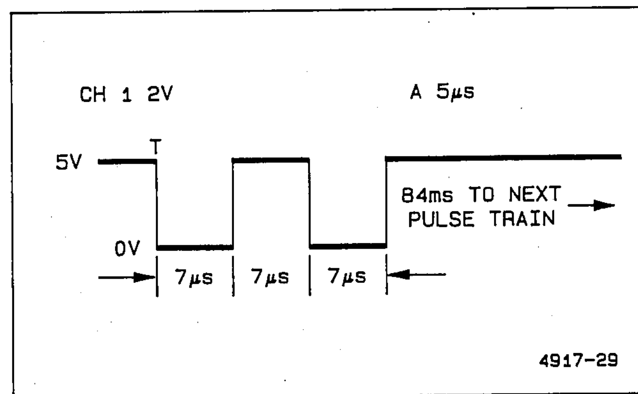

Figure 6-9. Front Panel μP diagnostics test.

3. If the test waveform is not present and the supply voltage, the ground, and the clock are correct, change the Front-Panel μP; it is possibly defective.

If the Front-Panel μP checks out ok, turn off the power and remove the jumper connected for the preceding Front Panel diagnostic test. Turn the scope back on and perform the following circuit checks for any of the Front Panel tests that failed when running the Extended Diagnostics via the GPIB. Use the circuit checks to isolate the problem in the associated circuitry. IF THE FPP DIAGNOSTICS TEST FAILED, THE ONLY WAY TO RUN THESE TESTS WILL BE VIA GPIB, AS THE FRONT PANEL WILL NOT RESPOND TO BUTTON PRESSES. To gain access to the scope via the GPIB when the EXT DIAG menu is being displayed, a MENU OFF command must be sent to exit extended diagnostics.

Table 6-6 (cont)

NOTE

Since the Front Panel μP is being reset in this test, there is no way to HALT if one chooses a CONTINUOUS loop mode and runs the tests from the front panel. However, to allow access to these features for any possible troubleshooting, looping has not been disabled. ONCE A TEST IS INVOKED IN CONTINUOUS MODE, A POWER OFF/ON CYCLE MUST BE USED TO EXIT FROM THE FRONT PANEL. Via the GPIB, the tests may be started and halted by sending the appropriate commands.

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Run tests 4100 through 4600 in CONTINUOUS mode. Use the CH 2 probe for the following checks while the specific test is selected and running.

4100 A13U861 pin 9 (FPINT):

1. Check U862 pin 1 for 0.2 μs negative strobe during the HI period of the trigger strobe. If not present, replace U862.

2. Check U861 pin 9 for a HI-to-LO transition. If not occurring, replace U861.

4200 A13U861 pin 6 ($\overline{\text{FPDNRD}}$):

1. Check U861 pin 1 for a negative strobe during the HI period of the trigger strobe. If not present, replace U862.

2. Check U861 pin 6 for a LO-to-HI transition from the strobe at U861 pin 1. If occurring, replace U861.

4300 A13U700 pin 12 (WR TO HOST):

1. Check that U861 pin 9 has a HI pulse. If not, select 50 ms/div and ENVELOPE acquisition mode on the test scope; then, run test 4000 for the scope under test. At pin 12 of U700, check for a strobe occurring near the falling edge of the trigger strobe. If the strobe is ok, replace U861. If missing, test for 4 MHz at U700 pin 5 and replace U700 if the 4 MHz clock is ok.

If the 4 MHz clock is missing, troubleshoot the clock source. Restore the prior test scope setup as for test 2110 (a good use for the AUTOSTEP SEQUENCER).

4400 DIAG BYTE A13U700:

1. Check that the enable pulse to U751 (pins 1 and 19) is present and save to REF1. If not present, check for an open between U862A pin 1 and U751 pins 1 and 19.

2. Display REF1 and probe U751 pin 18, 16, 14, and 12. These should all be LO during the time U751 is enabled. If not LO, it indicates either a problem in U700 or an invalid DC voltage level at one of the U700 inputs. If one of these four diagnostic bits is HI and the supply pins, etc., are ok, replace U700.

4500 A13U700 pin 13 (FPDNRD):

1. Select the 1/2 TRIG POSITION and set the Sec/Div setting to 1 ms on the test scope. Check for the FPDNRD clock pulse to U861 at pin 3 (leads the trigger strobe rising edge about 120 μs). If missing, replace U700.

Table 6-6 (cont)

	2. Check for LO at U861 pin 6; replace U861 if pin 6 is HI. 3. Check A12U654 pin 13 for LO. Replace A12U654 if pin 13 is LO and test is failing.
	4600 A13U742/A13U751: 1. Check for a pattern of 10100101 at U742 pin 19, 16, 15, 12, 9, 6, 5, and 2 at the rising edge of the trigger strobe (Word Recognizer Probe is useful for this check). If not, and U742 pin 11 is LO, then replace U742. If U742 pin 11 is HI, replace U700. 2. Check the enable pulse at U751 pins 1 and 19. Save and move to REF1. 3. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at U751 pins 17, 15, 13, 11, 8, 6, 4, and 2. If not ok, replace U700. 4. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at U751 pins 3, 6, 7, 9, 12, 14, 16, and 18. If not ok, replace U751.
4700 BATT STATUS	Battery A12BT800 (NVRAM keep-alive battery) (schematic diagram 1): Testing Method: There is no hardware exercised for this test. The operating system is informed by the front panel processor if the battery voltage is either high or low. The "test" is to read a memory location where the System μP has stored the status after checking with the FPP. If the status is unknown, the result is NULL. If the test "passes," it means that it is not defective in that direction.
	Troubleshooting Procedure: 4710 HIGH: Either the voltage is really high or the detection circuitry is defective. 1. Measure the battery voltage directly across the battery (BT800) and check for a range of 2.5 V to 3.7 V. If ok, then test from the + lead of BT800 to ground for the same or less voltage. 2. If ok, test for the same voltage range at A13U700 pin 21. If ok there, replace A13U700. If voltage is wrong at pin 21, backtrack to the problem component (suspect A12U940). 3. If the battery voltage is too high or the voltage to ground from the + lead is too high, check A12CR802. To ensure continued proper operation of the NVRAM, replace A12BT800 after correcting the overvoltage condition. **WARNING** *When replacing the lithium battery, avoid personal injury by observing proper methods for handling and disposal. Improper handling may cause fire, explosion, or severe burns. Don't attempt to recharge and don't crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* 4720 LOW: Either the battery is defective or the detecting circuit is defective.

Table 6-6 (cont)

	1. Measure the battery voltage for a range of 2.4 V to 3.7 V. If low, replace the battery (BT800) observing the proper handling procedures. 2. If the battery voltage is correct, troubleshoot the detection circuitry as for a failure of test 4710, looking for the cause of a LOW reading.
5000 WP U470	Waveform μP A12U470 (schematic diagram 2): Testing Method: The nature of these tests is such that all tests must be executed in order and may not be individually executed. Therefore, any attempt to execute one test will result in all tests being executed. The Waveform Processor test first sets all test results to NULL. Any failures will be fatal in terms of instrument operation; however, the last test that was executed will be set FAIL and should help in diagnosing the cause of the problem. The Waveform μP command memory has been checked out by this time as well as the bus structure that permits the System μP to control the Waveform μP bus.
5100 RUN-TASK	Testing Method: Loads a task into Command Memory U440 and tells the Waveform μP to execute it. A 30 ms timeout is executed; and then, INTREG (bit 0) is tested for WPDN. If it has not been set, the task did not execute and terminate properly. If 5100 fails, it could be the Waveform Processor code ROMs, or the Waveform μP itself (U470). In any event, the Waveform Processor Kernel tests will need to be run to diagnose the source of the problem. Troubleshooting Procedure: Use the Waveform μP Kernel test in Procedure 8 to troubleshoot for a μP fault or a fault on the Waveform μP address or data bus.
5200 BUSGRANT	Testing Method: This test executes a bus request by setting bit D5 (pin 14) of PCREG U860 (schematic diagram 1) HI, delaying 10 ms, and checking bit D6 of INTREG (Interrupt Register) U654 to see if a BUSGRANT has occurred. Troubleshooting Procedure: Set up the 2440 test scope as in Step 1 of the 2110 troubleshooting procedure. Run test 5200 in CONTINUOUS mode. Using the CH 2 Probe: 1. Check U860 pin 15 for LO-to-HI transition. If not occurring, replace U860. 2. Check U332D (schematic diagram 2) pin 13 for LO-to-HI transition. If not occurring, replace Waveform μP U470. 3. Check U332D pin 11 for LO-to-HI transition. If not gating, replace OR-gate U332.

Table 6-6 (cont)

5300 VERSION-CHK	Waveform μP ROM A12U480 and A12U490 (schematic diagram 2): Testing Method: The version number in the header is preset to "?" and is filled in by this test. If the test fails, the "?" will remain in the header for further indication of an error. A Waveform μP reset causes the Waveform μP to read the version number bytes of the Waveform μP code. If the version number is incorrect, the Waveform μP code is incompatible with the System μP code and may not execute properly. Troubleshooting Procedure: If test 5300 fails, replace Waveform μP ROMs U480 and/or U490 with the correct ones for the version of System μP code being used.
6000 CK SUM-NVRAM	Nonvolatile RAM Checksum A12U664 (schematic diagram 1): Testing Method: Some of the CRCCs (check sums) are computed at power-down and will be valid only at power-up. Therefore, executing tests 5000 through 5003 will only display the flags that resulted from power-up diagnostics. *NOTE* *FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test ran. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.* When the instrument is SELF CALIBRATED, a CRCC is calculated and stored for the Calibration Constants in NV RAM. When power-down is executed, the values of the front-panel variables have a CRCC calculated and stored. When a waveform is saved, the CRCC is calculated for the waveform and headers and saved. On power-up, all of these are recalculated and compared to the stored CRCC word. If they do not agree, that test fails.
6100 CAL CONSTANTS	Calibration Constants: Troubleshooting Procedure: If FAIL, the calibration constants have been lost and a COLD START is executed. The instrument must be recalibrated to return to calibrated operation after a COLD START. A failure of 6100 is serious to the normal operation of the scope, and the cause of the failure should be found and corrected to prevent reoccurrence. 1. Check BT800 and the components that connect and disconnect the battery from the NV RAM at power-off and power-on respectively.

Table 6-6 (cont)

	WARNING *If replacing the lithium battery, avoid personal injury by observing proper methods for handling and disposal. Improper handling may cause fire, explosion, or severe burns. Don't attempt to recharge and don't crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* 2. Test several times by cycling the power after the instrument has completed its self testing. If the test continues to fail, check the PWRUP line to U640 pin 2, and ensure that it is reset LO when the power line voltage drops below the minimum line voltage. If this line does not go LO soon enough, the power-down routines will not calculate the current check sums before the power is completely lost.
6200 FP-LAST	Front Panel Control Settings: Troubleshooting Procedure: If the last front-panel setup has been lost, the instrument will be set up in the INIT PANEL configuration in the AutoStep Sequence menu (push PRGM). If this event is due to a component failure, the RAM test, 3700 and/or 3800, or BATT-STATUS test 4700 should also have failed. Check NVRAM device U664 and associated circuitry or the Battery circuit as appropriate. The reference waveform memories will be declared EMPTY if the WFM-HEADERS do not check correctly. These waveforms are stored in A12U350. Therefore, if the problem is due to failed components, the RAM test (3300) or BATT-STATUS (4700) should have failed.
6400 PRGM	State of the AutoStep Sequencer memory: Testing Method: Each time an AutoStep Sequence is modified, a CRCC (check sum) is calculated and stored. At power-up, a CRCC is calculated again and compared with the last value stored. If there is a discrepancy, the FAIL flag is set and all the pointers for the AutoStep Sequences are initialized so that the sequences are lost. The most likely cause of a PRGM failure is a loss of power while memory is being reclaimed after a sequence has been deleted. If, rather, this event is due to a component failure, the RAM test, 3700 and/or 3800, or BATT-STATUS test 4700 should also have failed. Check NVRAM device U664 and associated circuitry or the Battery circuit as appropriate.

Table 6-6 (cont)

7000 CCD	CCD/CLOCK DRIVERS A10U350 (CH 2) and A10U450 (CH 1) (schematic diagram 10): Testing Method: These tests, if passed, indicate that the hardware is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. The CCD has two classes of adjustments, centering and gain. In addition, several CCD parameters are measured and stored for use in Dynamic Calibration. Centering must be performed in all four acquisition modes because of offset differences in the different paths. Gain is performed in Short-Pipeline and FISO modes.
	Troubleshooting Procedure: The CCDs are a good suspect if any of the 7000-series diagnostic tests failed. The Extended Diagnostics menu should be examined to determine if the problem is in only one or in both of the channels. If both channels fail: 1. Check the CCD clocks. To determine if a clock problem is internal or external to the CCD/Clock Driver hybrid, compare the collector voltages of Q450 and Q460 to Waveform illustration 67 (associated with schematic diagram 10). If either of the clock waveforms is different, check the base of the associated transistor(s). If the base voltage is switching correctly, change the defective transistor. If not switching, trace back to the clock source from U470, the Phase Clock Array (on diagram 11), and check there. If the clocks are not correct there, change U470. 2. If the clocks are running correctly at the collectors of Q450 and Q460, check to see if pins 2, 3, 5, and 6 of R470 are switching correctly (compare pins 2, 3, 4, and 5 to waveforms 68 through 71 on diagram 10). If not switching correctly, check the outputs of U470 for correct clock. If not present there, troubleshoot the Phase Clock Array (U470); if ok there, find the open. If a single channel fails: 1. Change the associated CCD/Clock Driver U450 or U350. If the problem is not corrected, troubleshoot the CCD Output circuitry. *NOTE* *If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the ±2 division gain for the changed channel both Side 1 and Side 2 according to the directions given in the display.*

Table 6-6 (cont)

CCD Output Troubleshooting Procedure (Schematic Diagram 14):

NOTE

Steps 1-6 troubleshoot only that section of the CCD OUTPUT (schematic diagram 14) that processes the plus/minus signal pair (CCDO11+/CCDOD11−) that is output by side 1 of the CH 1 CCD. The references to components and signals in these steps only apply to that channel and side. *See schematic diagram 14 to determine the corresponding components for troubleshooting the sections processing the remaining signal pairs for CH 1 CCD side 1 (CCDOD12+/CCDOD12−, CCDOD13+/CCDOD13−, and CCDOD14+/CCDOD14−), and those for the CH 2 CCD side 2 (CCDOD21+/CCDOD21−, CCDOD22+/CCDOD22−, CCDOD23+/CCDOD23−, and CDOD24+/CCDOD24−).*

1. Input the 2440 calibrator signal to the channel that is not operating properly. If neither is working, start with CH 1. (CH 1, side 1 components are referenced; see NOTE above.) Set the bad channel to 100 mV/div, DC coupled, with 50 Ω termination off. Adjust the screen waveform so the ground dot on the scope under test is 2 divisions below center screen if possible. Set the input coupling of the other channel to ground. Turn the A SEC/DIV to 5 μs.

2. Verify that pin 3 (CCDOD11+) of A30 (Gain Cell Board) looks similar to waveform 104 (on schematic diagram 14), with center screen being at +5 V. If this waveform does not appear, troubleshoot the CCD/Clock Drivers. Verify that pin 2 (CCDOD11−) of A30 resembles waveform 105. Again, if this waveform does not appear, go to the CCD/Clock Driver troubleshooting.

3. Examine pin 18 of A30. The waveform here should have an offset of +7.5 V, which is shown at center screen on waveform 106 for diagram 14. If this waveform does not look right, check the components on A30 for failures.

4. Compare pin 1 of A30 to waveform 107. If this waveform does not appear, check to see that pin 3 of U560 is switching between 0 and +15 V; if it is, then the switch (U560) is bad. If it is not switching, check to see if the base of Q660 (Q670) is switching between 0.5 V and 0 V; if it is, the transistor is bad. If it is not switching, trace $\overline{\text{OSAM1}}$ back to the Time Base board.

5. Observe the waveform at pin 1 of U770. It should be similar to waveform 110, except that an offset of up to ±1.3 V may appear. If this is not the case, check the +10 V_{RA} supply and the centering voltage (7.5 V ±1.3 V). If the voltages are correct, check U770 and its associated transistors and other components for failure.

6. Check the collector of Q773. It should look like waveform 109, where center screen corresponds to ground; if not, check that the base of Q773 is switching on and off. If base is switching but the collector is not, check the transistor for a collector-to-emitter short. If it is not switching on the base, trace the $\overline{\text{MS11}}$ signal back to the Time Base board. The timing relationships of the $\overline{\text{OSAM}}$ and the $\overline{\text{MS}}$ signals are shown in waveform 45 through 51 of the System Clocks schematic (diagram 7).

Table 6-6 (cont)

7300 EFFICIENCY	CCD/CLOCK DRIVERS A10U350 and A10U450 (schematic diagram 10): Testing Method: This test measures the transfer efficiency of the CCD by comparing the gain of columns 2 and 16 of the CCD B register arrays. To do this, a ±4 division input is applied to the Peak Detector calibration inputs and acquired. Efficiency loss and apparent offset for the gain are both calculated and stored for use in dynamic data correction. Efficiency loss of more than 6% will cause an error to be flagged. Testing is performed at two SEC/DIV settings (2 μs and 500 ns) on all four CCD channels. Troubleshooting Procedure: If all other tests are ok, the most probable cause of failure is a defective CCD; replace the failed CCD.
7400 PD-OFFSET	PEAK DETECTORS A10U340 (CH 2) and A10U440 (CH 1) (schematic diagram 10): Testing Method: This test is to check the match of the offsets of the two paths through the peak detectors. A 0 V cal signal input (DAC value = 2048) is acquired and the A and B peak detector and D and C peak detector pairs (see Figure 3-5 in Section 3 of this manual) are matched by iteratively adjusting the appropriate PDOS (peak-detector offset) DACs and remeasuring the difference until offsets are matched. If matching cannot be accomplished within 1/2 DL for calibration or 1 DL for diagnostics, the test terminates due to acquisition count, and the test result is set to FAIL; otherwise, it passes. The SPECIAL menu choices under Extended Functions provide a diagnostic switch to divide the signal acquisition path. CAL PATH ON!OFF turns on or off the calibration signal path to the Peak Detectors. It is a useful diagnostics device in the event that large offset errors have driven the display off-screen. Switching CAL PATH ON eliminates the Attenuators and Preamplifiers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, then the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs. With CAL PATH ON, the FORCE DAC test may be used to check the operation of the Peak Detectors and CCDs using the CURS (CAL) adjustment. Troubleshooting Procedure: 1. Do a COLD START and use the FORCE DAC test to determine if the DAC system can control the PD-OFFSET voltages (PD11, PD13, PD21, and PD23) correctly. If not, troubleshoot the DAC system. 2. If the DAC system is functioning normally, the most probable cause of a failure is a faulty Peak Detector. Replace the Peak Detector of the failing channel NOTE *If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the ±2 division gain for the changed channel, Side 1 and Side 2, according to the directions given in the display.*

Table 6-6 (cont)

8000 PA	Preamplifiers A10U320 (CH 2) and A10U420 (CH 1) (schematic diagram 9): Testing Method: The PA tests, if passed, indicate that the analog acquisition circuitry is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. The Preamplifier has constants for Position Offset, Position Gain, Balance, Normal and Invert Gain, and Max Variable Gain. There is some interaction between adjustments. This effect is addressed by always using the previously stored constants in any setup and executing SELF CAL twice from a COLD START to assure an iterative solution of the calibration constants.
	Troubleshooting Procedure: 1. If SELF CAL fails, the calibration constants will most likely not be close enough to an operationally good value for the portions of the Preamp that work to function properly. Do a COLD START to replace the stored calibration constants with nominal values. *NOTE* *After a COLD START, the scope will need partial recalibration after it is repaired to return it to correct adjustment.* 2. If the 8000 level is flagged FAIL, there will be failure at one or more of the lower level tests. This is the case because one failure that misbiases the Preamp can cause several SELF CAL tests to fail. 3. After doing a COLD START, use the FORCE DAC test to determine if the DAC system can control the Preamp DAC voltages correctly for the tests that are flagged FAIL. Troubleshoot the DAC system for those DAC outputs showing no or improper control. 4. Check that the Preamp is responding to the DAC control voltage being changed. These are respectively for CH 1 and CH 2: 1POS and 2POS to pin 17 for position input. CH1G and CH2G to pin 18 for gain control. CH1B and CH2B to pin 2 for balance.

Table 6-6 (cont)

The check is set up by first doing a COLD START (to again set the calibration constants to known values), and then applying a 4-division signal to the CH 1 and CH 2 vertical inputs (or to the bad channel if only one is bad). Observe the signal on the crt, if possible; otherwise, use a test scope to probe the vertical signal path to check for correct response. Since the Preamp outputs are not accessible, use the output of the Peak Detectors to verify the signal through the Preamp. The side 3 Peak Detector output for CH 1 may be checked on R441 and R540; and for the CH 2 side 3 output, check at R244 and R341.

Use either the Front Panel Controls or the Force DAC test to check the VARIABLE GAIN and VERTICAL POSITION. Balance may be varied only using the Force DAC function. Varying the channel balance should appear as a dc offset change to the vertical signal level. Prior to making any adjustments after a COLD START (either with the Front Panel controls or the Force DAC function), the signal at the output of the Peak Detectors should have a +8.7 V dc level with an ac signal (replica of the input signal) of approximately 0.5 V peak-to-peak.

5. The Preamplifier operating mode is set by a serial data word sent from the System μP. The CD input, pin 22, is the serial data input. A TTL-level logic swing should be present on this line whenever the Attenuators, Preamps, or A/B Trigger Generator operating modes are being set up. If there are no FAIL flags under these major test categories, the CD circuitry is most likely functioning properly. The $\overline{CC}$ input, pin 23, is the control clock input, and it should have a TTL-level logic swing on it only when the particular hybrid, in this case the Preamp hybrid, is being set up. Check that this line is high initially and pulses LO eight times for each Preamp load cycle. (The eight pulses may be separated into several groups of pulses.)

6. The Preamps have bypassed and decoupled voltage supplies. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.

7. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.

Table 6-6 (cont)

8100 POSITION OFFSET	Acquisition System Position Offset: Testing Method: Position Offset is calculated at 50 mV per division only. Position offset must be performed for all four acquisition modes to compensate for the common-mode offsets in the CCD arrays that are not corrected by CCD centering. After the hardware is set up and the CCD constants set for the particular mode of operation, the Preamplifier is balanced by executing the balance routine, but only changing the DAC settings—not the cal constants. This assures an accurate position measurement. The Position Offset is then calculated by acquiring a ground level signal and comparing the Acquisition Memory value to what a ground acquisition should be (center screen is 00h). If the value is not within 1/2 DL for calibration or 1 DL for diagnostics, the position DAC outputs (CH1-PA-POS and/or CH2-PA-POS) are adjusted to compensate. When the acquisition is within limits, the test result is set to PASS. If the position offset cannot be adjusted to within specification, the acquisition count for an abort is taken, and the test result is set to FAIL. Troubleshooting Procedure (refer to test 8000 for more information): 1. Check that the decoupling network, R420/C423 or R222/C222 is functional. 2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or CH2-PA-POS voltages are being controlled by the DAC System. If not, troubleshoot the DAC System. 3. Use the SPECIAL menu choice of CAL PATH ON to determine whether the offset error is prior to the Peak Detectors or after. Troubleshoot in the appropriate direction to locate the source of the offset error. 4. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 5. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 6. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.
8200 POSITION GAIN	Preamplifier Position Gain A10U420 and A10U320 (schematic diagram 9): Testing Method: Position Gain is calculated at 50 mV per division only, using the stored Position Offset calibration constant. The DAC counts corresponding to +4 divisions of Position Offset are added to the Position Offset constant and an acquisition is made. After storing the results, a corresponding −4 division acquisition is made, and the two values of acquisition memory are checked for eight divisions of change in the calibration limits. The Position Gain constant is then calculated as a result of the data taken and stored as a Position Gain calibration constant. A Position Gain constant more than 20% different from the nominally expected value will cause the test to fail. *NOTE* *POSITION GAIN is not an iterative calibration as the gain is directly calculated.*

Table 6-6 (cont)

	Troubleshooting Procedure (refer to test 8000 for more information): 1. Check that the decoupling network, R420/C423 or R222/C222 is functional. 2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or CH2-PA-POS voltages are being controlled by the DAC System. If not, troubleshoot the DAC System. 3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 4. If the Preamp hybrid itself is suspected to be defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.
8300 PREAMP BALANCE	Preamplifier Balance A10U420 and A10U320 (schematic diagram 9): Testing Method: Balance is performed in all five Preamplifier ranges, and on both channels simultaneously. Balance is calculated by first taking a ground acquisition in non-invert. Then an acquisition is made in INVERT, and a new balance DAC voltage is calculated that will keep the trace shift between non-invert and INVERT within limits for calibration or diagnostics. This is done until balance is within specification or until the maximum number of acquisitions has been reached. If the result is within specification prior to acquisition abort, the test result is set to PASS; otherwise, it is set to FAIL. Balance Test Limits: Range: 50 mV / 20 mV / 10 mV / 5 mV / 2 mV Cal limit: 1/2 DL / 1/2 DL / 1 DL / 1 DL / 2 DL Diag limit: 1 DL / 1 DL / 2 DL / 2 DL / 4 DL
	Troubleshooting Procedure (refer to test 8000 for more information): 1. Check that the biasing network associated with the balance input, pin 2, and pins 4, 20, and 25 is functional and that the voltage levels are approximately those indicated on the schematic diagram in the service manual. 2. Use the FORCE DAC test to determine if the CH1-BAL and/or CH2-BAL voltages are being controlled by the DAC System. If not, troubleshoot the DAC System. 3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 4. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

Table 6-6 (cont)

8400 PREAMP GAIN and 8500 PREAMP INVERT GAIN	Testing Method: During calibration, gain constants are computed by using the Balance control to position +2.5 and −2.5 divisions and computing the next gain DAC value until the result is set to be within specifications. For diagnostics, the swing is reduced to ±1.5 divisions to allow for thermal drifts that occur due to temperature changes between power off and power on. The effects of thermal drift are especially noticeable at high vertical sensitivities. Limits are 1 DL for calibration and 2 DL for diagnostics. Gain is done for all five Preamplifier ranges in both normal and invert modes. Both Preamplifier channels are tested simultaneously. Since the transfer function of the gain control is non-linear, correction is done iteratively either until the gain is within specifications or until the maximum number of acquisitions allowed for the test has been reached. If the result is found prior to a test abort, the test result is set to PASS; otherwise, it is set to FAIL.
	Troubleshooting Procedure (refer to test 8000 for more information): 1. COLD START and use the Force DAC test to check that the DAC system is controlling the CH1-GAIN-CAL and CH2-GAIN-CAL voltages correctly. If not ok, troubleshoot the DAC system. 2. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual. 3. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact. 4. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.
8600 PREAMP VAR MAX	Testing Method: In this test, the change in Preamplifier control which will yield an attenuation of 2.75 from the Calibrated VOLTS/DIV setting is measured on both channels at 50 mV per division in normal mode. This is done by re-performing the 50 mV noninverted gain test seeking a value of +2.5 divided by +2.75 (+0.91) division and −2.5 divided by −2.75 (−0.91) division on the output. The difference between the resulting gain control DAC setting and the gain control DAC calibration constant is the Var Max value. Inability to achieve an attenuation factor of 2.75 is a test failure.
	Troubleshooting Procedure (refer to test 8000 for more information): See the Troubleshooting Procedure for tests 8400 and 8500.

Table 6-6 (cont)

8700 ATTENUATORS

Channel 1 and Channel 2 Attenuators AT400 and AT300 (schematic diagram 9):

Testing Method:

THIS TEST IS ONLY PERFORMED USING EXTENDED CALIBRATION. With the Preamplifier set to 50 mV non-inverted, the Preamplifier gain test is repeated interactively using standard dc test voltages applied to the CH 1 and CH 2 inputs. By adjusting the Preamplifier balance to give −2 divisions, the output is swung between −2 (input grounded), and +2 (input set to 0.2 V per div), divisions. The gain control DAC is adjusted to achieve an output within specifications. The difference between the resulting control DAC setting and the gain calibration constant measured at 50 mV per division (non-inverted) is the attenuator gain constant. If a solution cannot be found, or if the resulting solution is more than a 2% gain error, the test result is set to FAIL. If the test fails, an attenuator gain of 0 (nominal) is stored for the calibration constant under the assumption that the test setup may be in error. The test is repeated for all three vertical attenuators (1X, 10X, and 100X) using input test voltages of 0.2 Vdc, 2 Vdc, and 20 Vdc.

Troubleshooting Procedure:

1. Check that the correct test voltages are used for the ATTEN calibration step.

2. Check that one audible click is heard when changing the VOLTS/DIV setting between 50 mV and 100 mV (10X attenuation) and between 500 mV and 1 V (100X attenuation). Also check that one audible click is heard when changing the Vertical input coupling between DC and AC, and when turning the fifty ohm input ON and OFF. Several clicks will normally be heard when switching in and out of GND Coupling.

3. If one and only one audible click was heard for each of the first four front-panel changes above, then the circuitry that drives the four mag-latch relays in each attenuator is functioning properly by switching the individual relays to the opposite latched position (the audible click).

4. Connect the output of a Standard Amplitude Calibrator to the vertical input of the failing channel using coaxial cable with no terminator. Set the Standard Amplitude Generator output and the VOLTS/DIV setting on the scope to the values given in the following table and check the signal path between the Attenuator and the Preamplifier input of the failed channel. With a 10X probe on the test scope, view the signal at the Preamp input pin. Use NOISE REJ Trigger Coupling and 20-MHz Bandwidth on the test scope to clear up the trace noise and obtain a stable trigger. If only one channel is bad, the other channel of the scope may be used to view the signal. The signal amplitude out of the Attenuator and into the Preamp should be approximately 50 mV peak-to-peak for each attenuator setting in the three ranges. A possible, but unlikely, source of a failure that is not in the signal path between the Attenuator and the Preamp is a shorted capacitor (C414 or C311) connecting to the Attenuator.

ATTENUATOR CHECK

Signal In	VOLTS/DIV	Signal Out
50 mV	2 mV to 50 mV	50 mV
0.5 V	100 mV to 500 mV	50 mV
5 V	1 V to 5 V	50 mV

5. If one channel shows PASS flags on all the ATTEN tests, swap the Preamps between channels to determine if the Preamplifier inputs are ok. If that swaps the problem, replace the faulty Preamp. If the problem remains in the same channel, replace the defective Attenuator.

Table 6-6 (cont)

	6. If none or only some audible clicks were heard, and assuming the Attenuator Register and Preamplifier tests passed the Power-on SELF TEST or a subsequent EXTENDED DIAGNOSTIC test, troubleshoot the magnetic-latch buffers (U510 and U220) and the latching circuitry (Q620, Q621, U520, and associated components) on diagram 9. 7. Check the ATTEN CLK line for the presence of a signal at the times when an audible click should be heard. 8. Shift Registers U221 and U511 are assumed functional with proper input signals if there is a PASS flag present at the 2520 level of the Extended Diagnostics menu after performing the EXT DIAG diagnostics test. Otherwise, troubleshoot the Shift Registers for the source of failure.
9000 TRIGGERS	A/B Trigger Generator A10U150 (schematic diagram 11): Testing Method: The Triggers tests, if passed, indicate that the analog trigger circuitry is functional. IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests. Whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution. Triggers have constants for offset and gain. The value of Level DAC output that caused the trigger to change state is assumed to be the upper hysteresis level in plus slope and the lower hysteresis level in negative slope. *NOTE* *TRIGGER MODE is set to A and B to program ATG output to be the AND of A and B triggers. Thus ATG may be tested as an indication that triggering has occurred. This requires that BOTH A AND B TRIGGERS MUST BE FUNCTIONAL TO GET EITHER TEST RESULT TO PASS.* Troubleshooting Procedure: External and Internal Trigger Path (common circuitry): 1. For this test to result in a PASS flag, several major circuit blocks must work correctly. Common to both the external trigger signal path and the internal trigger signal path is A/B Trigger Generator A10U150 (schematic diagram 11) with the following related input signals: a. ATHO (A Trigger Holdoff) from the Trigger Holdoff circuit (schematic diagram 13) to A/B Trigger Generator U150 through a level shifting resistor string of R225 and R134. The level at U150 pin 15 is less than +3.3 V for logic LO and greater than +4.0 V for logic HI. The input must be logic HI for a trigger output to occur. If the ATHO signal is not correct, see the "HOLDOFF PROBLEMS" in Procedure 4. b. A TRIG LEVEL and B TRIG LEVEL from the DAC System (schematic diagram 6) via A10U640A (A TRIG LEVEL) and A10U640D (B TRIG LEVEL) and filter networks R250-C250 or R162-C160 is another. These voltage levels should be adjustable from −1.3 V to +1.3 V using the FORCE DAC function.

Table 6-6 (cont)

c. ACD (Acquisition Control Data), A TRIG CLOCK, and B TRIG CLOCK are the signals that load the internal shift register of U150 with MODE, CPLG, and SLOPE requirements for the trigger signal. These lines should have TTL level voltage swings, and the A TRIG CLOCK clock and B TRIG CLOCK signal lines should only have transitions when the associated A or B Trigger MODE, CPLG, or SLOPE are changed. The ACD data line (U150 pin 46) should be checked for the presence of voltage transitions.

d. Six $\overline{\text{SR}}$ data lines set up the A TRIG SOURCE and B TRIG SOURCE selections. Shift Register A10U140 (schematic diagram 5) provides these signals, and it is tested by test 2510 of the Extended Diagnostics. The signals are assumed correct for a PASS flag at that diagnostic level. If a FAIL flag is present, follow the Troubleshooting Procedure under that diagnostic level.

2. High speed ECL level shift stages, Q250 and Q251 for MAIN GATE and Q150 and Q151 for DELAY GATE, are common paths for both Internal and External trigger sources. These stages should have an ECL input swing of less than +3.4 V for logic LO and greater than +4.0 V for logic HI. The output swing should be greater than −1.6 V for logic LO and less than −1.1 V for logic HI.

3. Trigger Logic Array A10U370 is also common to both the external and internal trigger signal paths. Related signal inputs that must be correct are:

   a. EPTHO (End Pretrigger Holdoff) from Timebase Controller A11U670 (schematic diagram 8) via buffer U680E on the Timebase board. EPTHO must be TTL high for a trigger to occur. If that is not occurring, see the Timebase and System Clocks troubleshooting chart in the Diagrams pages at the back of this manual.

   b. $\overline{\text{WR}}$, $\overline{\text{ACQSEL}}$, A0-A3, and GAD0-GAD7 are the digital control and data lines. These signals are tested by test number 2510 of the Extended Diagnostics and, if a PASS flag is present, are assumed to be correct. Otherwise refer to that diagnostics troubleshooting procedure for a failure of 2510.

4. The ATG path from Trigger Logic Array U370 to data bus bit D0 is also a common path. The AND logic function of the A Trigger Gate and the B Trigger Gate is performed within Trigger Logic Array U370. The path from A/B Trigger Gate inputs, through a logic ANDing gate, to the Trigger Logic Array Output (pin 63, ATG) is asynchronous and direct, delayed only by the propagation delay of the internal logic gate structures. The ATG signal has a TTL voltage level swing. The ATG output signal path is through R368 and W110 to buffer U851C (schematic diagram 13) and then through tristate buffer U761 to the D0 bit of the System μP data bus. This path through buffer U761 is not tested by test 2000 (Register Tests) of Extended Diagnostics, so it must be verified from U370 through U761 to be operational. ATG also clocks Trigger Holdoff flip-flop U872A.

EXTERNAL TRIGGER PATH—EXCLUSIVE:

5. EXTERNAL TRIGGER PREAMP A10U100 (schematic diagram 9) is only in the External Trigger Signal path. It should be verified to be functional if FAIL flags appear only at Extended Diagnostics levels with EXT labels.

   a. There are only two mode control bits that set up U100. These bits are assumed to be correct if level 2510 of Extended Diagnostics shows a PASS flag. These two bits set up the 1X or 5X attenuation for each EXT TRIG channel.

   b. Q110, U120, and associated circuitry produce a +5 V source that tracks the instrument −5 V source. The voltage level at U100 pins 17 and 44 should be verified to be +5 V. The decoupled −5 V power supply voltage at pin 7 of U100 must be present for this circuit and for the circuit of U100 to function properly.

Table 6-6 (cont)

c. The voltage at U100 pins 25 and 36 should be verified to be +5 V to test for defective decoupling components (L210/C211 and L120/C112).

INTERNAL TRIGGER PATH—EXCLUSIVE:

6. CH 1 and CH 2 PREAMPS U420 and U320, U230A, U230B, and associated components (schematic diagram 9) supply the Internal CH 1 TRIG and CH 2 TRIG signals, and should be verified for functionality if FAIL flags appear only on Extended Diagnostics levels with CH 1 or CH 2 labels.

   a. Operational Amplifiers U230B and U230A and associated components form common-mode level-trimming amplifiers for the CH 1 and CH 2 ±PICK outputs respectively. Since the CH 1 and CH 2 trigger signals originate from the −PICK outputs of the CH 1/CH 2 PREAMPs (U420 and U320), improper operation of these bias-trimming amplifiers will result in a diagnostic FAIL flag. When operating properly, the arithmetic average of the +PICK and −PICK bias voltages should be at or very near 0 V. If this is not the case, the amplifier circuitry needs to be repaired. (Note that the two circuits interact with each other.)

   b. If a channel PREAMP is suspected of having a defective −PICK output and the other channel shows no Diagnostics FAIL flags, swap PREAMPs to see if the problem moves to the other channel. If it does, replace the defective PREAMP.

9100 TRIGGER OFFSET	Trigger Signal Offset:

Testing Method:

A ground signal is provided to the trigger from the CH 1 or CH 2 pickoff (internal triggers) or from an external source (EXT1, EXT2 external triggers). This is done by grounding the attenuator or by providing a short at the EXT TRIG inputs.

The trigger level DAC is moved in two binary searches to determine where the upper and lower hysteresis levels are while holding the "other" trigger level in such a state that should be "triggered." The constant is then set to the hysteresis level that represents the triggering point for the desired slope at zero input. The test is repeated for both A and B triggers for all input paths. For EXT TRIG inputs, levels are measured for both the 1X and 5X (attenuated by a factor of five) amplifier ranges. An additional offset for the trigger slope is obtained by measuring the trigger in minus (−) slope with a CH 1 input and computing the difference between the obtained value and that measured in plus (+) slope.

Troubleshooting Procedure:

1. Run test 9100 in CONTINUOUS mode.
2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings.
3. Use the troubleshooting comments under 9000 level as a guide.
4. ATG signal should be present at TTL level voltage swings.
5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings.
6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: ±1 V swings, ±0.5 V swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done.

Table 6-6 (cont)

	7. CH1 and CH2 TRIGGER signals should be at or near 0 V. (LR421/LR220 can be open and not cause a FAIL flag to appear at this diagnostic test level since this test only requires CH1/CH2 trigger signal to be near 0 V, which is the case with these components open. However, a FAIL flag will appear at the 9200 diagnostic level.) 8. EXT1 and EXT2 TRIG signals are provided externally, and the external signal paths to the Trigger Source Select function within A/B Trigger Generator U150 are not tested by running test 9200 CONTINUOUS Mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional, and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.
9200 TRIGGER GAIN	Trigger Signal Gain: Testing Method: Trigger gain is measured for both A and B triggers and for CH 1 and CH 2 inputs. Trigger gain is set by positioning the input signal to +2 divisions using the CH 1 and CH 2 Preamplifier balance control. The trigger level is then determined by binary search using the same routine which is used for trigger offset. The same is done for −2 divisions. These results are then used to compute the trigger gain. Trigger Gain for the External Triggers is done in Extended Calibration of the TRIGGER circuits. A ground signal and externally supplied dc voltages are used to get a four-division level swing in both Ext Trig Preamp gain ranges. If gain cannot be measured, an error is flagged. On the External Triggers, a nominal gain value is stored if the test fails, on the assumption that the external setup may be faulty. The test(s) that failed will be marked FAIL in the Extended Diagnostic menu.
	Troubleshooting Procedure: 1. Run test 9200 in CONTINUOUS mode. 2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings. 3. Use the troubleshooting comments under 9000 level as a guide. 4. The ATG signal should be present at TTL level voltage swings. 5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings. 6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: ±1 V swings, ±0.5 V swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done. 7. CH1 and CH2 TRIGGER signals should have two levels separated by 100 mV centered approximately around 0 V. (LR421/LR220 can be open and cause a FAIL flag to appear only at this diagnostic test level while the 9100 TRIGGER OFFSET level shows a PASS flag since that test only requires CH1/CH2 trigger signal to be near 0 V, which is the case with these components open.) 8. EXT1 and EXT2 TRIG signals are provided externally and this signal path to the Trigger Source Select function within A/B Trigger Generator U150 is not tested by running test 9200 in CONTINUOUS mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.

Table 6-6 (cont)

9300 REPET	This routine is not a test. Enough samples are acquired to calibrate the Jitter Correction Gain in Extended Calibration.
	Troubleshooting Procedure: 1. Use the Jitter Correction Troubleshooting procedure to locate the source of the failure.
8	**DEAD START**
POWER SUPPLIES	Low Voltage Power Supply (schematic diagram 22) and Low Voltage Regulators (schematic diagram 23): 1. Test for proper voltages on the SIDE BOARD. Check +15 V, +10 V, +8 V, +5 V, +5 VD, −15 V, −10 V, −8.3 V (should measure −8.6 V), −8 V, and −5 V for proper levels. If any of the voltages are incorrect, troubleshoot the bad supply. The +5 VD supply is fused by F269 (schematic diagram 22) and the −15 V Unreg supply to the HV Oscillator is fused by F961 (schematic diagram 23). Both of these fuses are located under ribbon cables attaching to the power supply board and are hidden from view until the cables are disconnected. A Control Electronics Troubleshooting chart for the Low Voltage Power Supply is located in the "Diagrams" section of this manual. **WARNING** *If troubleshooting the Low Voltage Power Supply with the ac power connected, use of an isolation transformer is necessary to prevent damage to equipment and possible personal injury due to electrical shock.* 2. Check that PWRUP signal on U640 pin 2 (processor board) is HI and that the $\overline{\text{RESET}}$ signal on U640 pin 37 is HI after the power on. If not, troubleshoot the Power Up (schematic diagram 23) and Power Up Reset circuitry (schematic diagram 1).
PROCESSOR CLOCKS	System Clocks (schematic diagram 7): 1. Check System μP A12U640 pin 38 (schematic diagram 1) for 8 MHz. If not there, check System Clocks for the defective component(s) (schematic diagram 7). Check that J132 (40 MHz oscillator/External clock jumper, schematic diagram 7) is properly installed. 2. Check Front Panel Processor A13U700 at pin 5 (schematic diagram 3) for the 4 MHz clock. If not there, check System Clocks for the defective clock circuit (schematic diagram 7). 3. Repair clocks. Go to the System Clock Troubleshooting chart (located in the "Diagrams" section of this manual). 4. If clocks are working, and the scope still gives no signs of life, use the System μP Kernel Test to verify operation of the System μP addressing and chip-select circuitry.
SYSTEM μP	System μP Aborts on Start-Up or While Operating: There is some internal consistency checking that can result in an "abort" of the operating routines. The abort routine loops endlessly, blinking the Trigger LEDs on and off in an abort code. On an abort, the Trigger LEDs are flashed three times, then an abort code is displayed in binary with the TRIG'D LED being the LSB of the code (see Figure 6-5), and the cycle is then repeated continually.

Table 6-6 (cont)

In version 1.7 software, an abort will cause the Trigger LEDs to flash, but no coded flashing is done. The abort codes for version 2 software and possible causes of an abort are shown in the following table:

CODE	Meaning	Possible Cause
1	Abort code initialized to this value at power-on.	Bad ROM/RAM. Firmware bug.
2	Unknown code received from Front Panel μP.	Front Panel μP data path to System μP bad.
3	Too many bytes received from Front Panel μP.	Front Panel μP data path to System μP bad or handshake logic bad.
4	Software Interrupt 2 or Software Interrupt 3 instruction executed.[a]	Bad ROM/RAM. Firmware bug.
5	GPIB terminator value for query response scrambled.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)
6	GPIB event code to be reported is unknown.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)
7	GPIB delimiter found by scanner has changed and is invalid.	Bad ROM/RAM. Firmware bug. (May require a COLD START.)

[a]**SWI2 and SWI3 are not used in the software instructions. If executed, they were not as valid instructions.**

Use the System μP Kernel Test to verify the ability of the System μP to function.

System μP A12U640 (schematic diagram 1) Kernel Test:

1. With the power off, move jumper J126 from pins 1 and 2 to pins 2 and 3 of P126. This disables the System μP Data Bus Driver, and allows the data bus lines to be pulled up and down to a single-byte instruction. The instruction (CLRB) continually fetches and executes the CLRB instruction to step through the entire 64 K of addresses.

2. Move jumper J127 (Waveform Processor Bus control) from the NORMAL position (pins 1 and 2 connected) to the BUSTAKE position (pins 2 and 4 connected). This places the Waveform Processor Bus under control of the System μP. In the mode, the basic operation of the System μP can be checked, and all the address decoding circuitry can be verified.

3. Connect CH 1 of a test scope to TP840. Display that signal and use it as a trigger source for the test scope. This point is the AF address bit (the MSB) of the address bus.

4. Turn the power on and check that the $\overline{\text{RESET}}$ signal on U844 pin 8 is HI; if not, troubleshoot the Power Up Reset circuitry (schematic diagram 1) and the Power Up circuitry (schematic diagram 23).

5. Adjust the test scope to view the AF signal. It should be a TTL-level square wave with a 50% duty cycle.

Table 6-6 (cont)

Using the CH 2 probe:

6. Check each address line in order (from AF to A0) for a valid TTL-level signal, with each lower address line having a frequency of exactly twice the frequency as the address above it. Any loss of the 50% duty cycle and/or distortion indicates a shorted address line. Check both the input and output pins of Address Buffers U732 and U632 to verify that they are working correctly, and to determine if address lines are shorted after the buffers. Waveform numbers 6, 7, 8, 9, 10, and 11 on schematic diagram 1 may be used to compare against the observed waveforms.

7. If a fault is found, it may be necessary to isolate the System μP address bus from the Waveform μP address bus to determine what circuitry is causing the problem. See the BUS ISOLATE and the WAVEFORM μP KERNEL MODE procedures following the SYSTEM μP CHIP SELECT TEST.

System μP Chip-Select Test:

1. From the Kernel mode, momentarily short the pins of J129 together to reset the processor. This forces ROM0.0 to be switched in. Set the test scope to 10 ms/div to view one whole cycle of the AF period, and set the Trigger Slope so that AF is shown LO during the first half of the display. While AF is LO, addresses from 0000h to 7FFFh are being executed; while HI, addresses from 8000h to FFFFh are executed.

2. Move jumper J127 (shown on schematic diagram 2) to connect pins 2 and 4. This causes the "BUSTAKE" condition so that the System μP has access to the Waveform μP memory space. In this mode, most of the processing system can be verified.

Using the CH 2 probe:

3. Look for a LO chip-select signal, at the point designated in the following table, that occurs during the correct portion of the AF waveform period. Waveforms 20, 21, 22, 23, 24, and 25, may be used as comparison waveforms for the chip selects output from Address Decoder U570 (schematic diagram 2—Waveform μP).

Chip Select	Test Point	Bus	Address Range (hex)	Position Within the AF Period
$\overline{\text{SAVE}}$	U580-8	WP	0000-1FFF	First 1/8th
$\overline{\text{DISP}}$	U570-13	WP	2000-2FFF	Third 1/16th
$\overline{\text{DATT}}$	U570-12	WP	3000-3FFF	Fourth 1/16th
$\overline{\text{ACQ}}$	U570-11	WP	4000-4FFF	Fifth 1/16th
CMD/$\overline{\text{TEMP}}$	U250-8	WP	5000-57FF	Twelfth 1/32nd
$\overline{\text{COEFF}}$	U250-11	WP	5800-5FFF	Thirteenth 1/32nd
$\overline{\text{HMMIO}}$	U870-6	BOTH	6000-6FFF	Seventh 1/16th
NVRAM	U840-6	SYS	7000-77FF	Sixteenth 1/32nd
$\overline{\text{SYSRAM}}$	U840-3	SYS	7800-7FFF	Seventeenth 1/32nd
$\overline{\text{ROM0.X}}$	U890-4	SYS	8000-BFFF	Third 1/4th
$\overline{\text{ROM1}}$	U890-5	SYS	C000-FFFF	Last 1/4th

Table 6-6 (cont)

4. Check the host memory-mapped I/O selects at the outputs of U830 to verify that selects are generated and only during the time $\overline{\text{HMMIO}}$ is LO.

5. With the power off, check that no two of the select outputs are shorted together. If shorted, troubleshoot the cause and repair.

NOTE

If the problem is that one of the selects is not being generated, the SELF TEST will be able to determine that a group of registers fail. However, if two or more of the select lines are shorted together, any addressed devices will try to respond at the same time and bus contention will occur. The result is that the normal SELF TEST diagnostics testing won't work.

6. Check each of the System µP data bus lines (D7-D0) on the outputs of Data Bus Buffer U650. Look for open bus lines (no activity) and hung bus lines (stuck HI or LO). If a fault is found, it will be necessary to determine if it is on the System Bus or the Waveform µP bus. Use the BUS ISOLATE mode to assist in checking for a fault location.

BUS ISOLATE MODE

1. Move jumper J127 to the BUS ISOLATE position (pins 2 and 4 connected). This electrically disconnects the Waveform µP bus from the System µP bus to isolate the different parts of the processing system from each other.

2. Recheck the faulty data bus line to determine if it is still faulty (problem on the System µP data bus) or the fault is gone (problem on the Waveform µP data bus).

3. Check that no data bus activity is occurring during the Waveform µP address space (see Figure 6-10 to compare against). Faulty address decoding can cause response from an incorrectly addressed device.

4. Check that the data bus is at the "float" level during periods of inactivity (waiting for a response from devices that are on the Waveform µP bus). A HI or a LO in the idle period indicates a stuck data bus.

5. If no faults are found on the System µP data bus, the problem data line may be on the Waveform µP bus. Use the Waveform µP Kernel mode to check for faults while the busses are isolated.

Table 6-6 (cont)

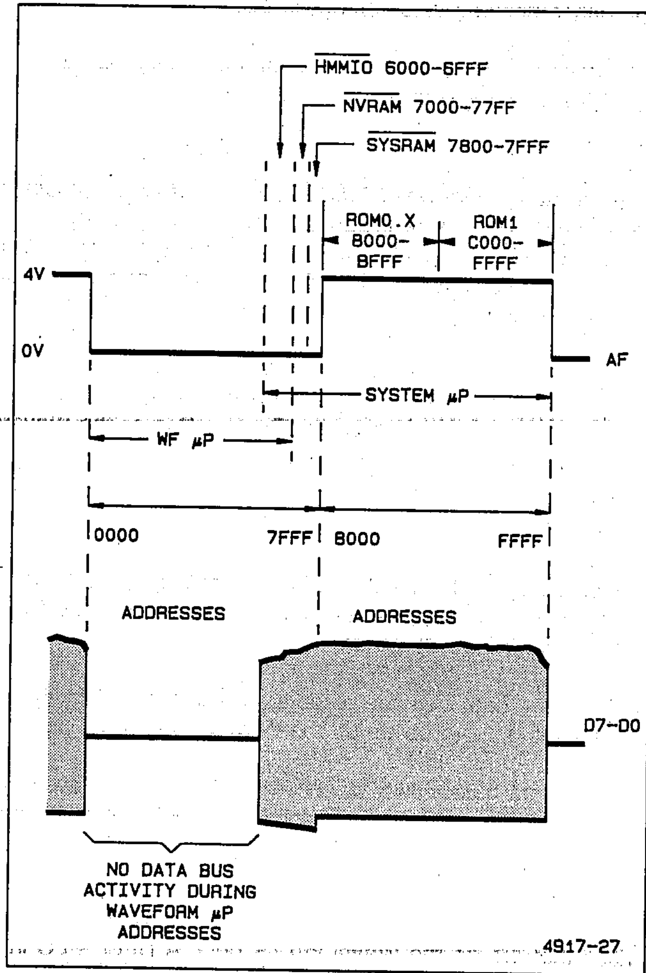

Figure 6-10. System µP data bit D7 in the Bus Isolate mode.

Table 6-6 (cont)

WAVEFORM μP

Waveform μP Kernel Mode:

This mode is used when a fault has been found on either the System μP data bus or the System μP address bus while in the BUS CONNECT mode or when SELF TEST 5100 (RUN TASK) fails in the Extended Diagnostics menu.

1. Turn off the power and place the processor system in the BUS ISOLATE mode (see the preceding steps).

2. Remove jumper J128 (Waveform μP Kernel Mode) and jumper 185 (Waveform μP Reset Release). Both are located on the Processor board near Waveform μP U470.

3. With the power on in the Kernel mode, the Instruction Data Bus lines are pulled up or pulled down in a command that causes the U470 to address every instruction in its memory sequentially and continually. Instruction address bus lines and data address bus lines can be checked for activity. All the Instruction address bus lines and the data address bus lines with the exception of the top five (WAA through WAE) increment with the periods shown in the following tables. WAA through WAE will be fixed random values because page switching of the memory is not done and is not set to any known state in the Kernel test.

Waveform μP Instruction Bus Address Lines

Signal	Location	Period
IA9	TP580	409.6 μs
IA8	U490-22	204.8 μs
IA7	U490-23	102.4 μs
IA6	U490-1	51.2 μs
IA5	U490-2	25.6 μs
IA4	U490-3	12.8 μs
IA3	U490-4	6.4 μs
IA2	U490-5	3.2 μs
IA1	U490-6	1.6 μs
IA0	U490-7	800 ns
CLK2D	U490-8	200 ns

Waveform μP Data Bus Address Lines

Signal	Location	Period
WAB	U562-9	1.6384 ms
WAA	TP562	819.2 μs
WA9	U562-5	409.6 μs
WA8	U562-2	204.8 μs
WA7	U364-19	102.4 μs
WA6	U364-16	51.2 μs
WA5	U364-15	25.6 μs
WA4	U364-12	12.8 μs
WA3	U364-9	6.4 μs
WA2	U364-6	3.2 μs
WA1	U364-5	1.6 μs
WA0	U364-2	800 ns

4. The Instruction Memory Data lines into the Waveform μP can also be checked to determine if any of the lines are shorted or open. Check against the schematic to see which lines (ID0 through IDF) are normally pulled up or normally pulled down for the Kernel test.

Table 6-7

Video Option Troubleshooting

VIDEO OPTION FAULT	Video Option (schematic diagram 21): If VIDEO is pressed and an error message of "VIDEO OPTION NOT INSTALLED OR FAULTY" is displayed, then the power-on SELF TEST has detected a problem (assuming the Video Option is installed). During the power-on SELF TEST, a byte is written to Line Counter A12U530 (schematic diagram 21) and read back. If the byte read back is not what is expected, a flag is set to indicate that the test failed. When the SET VIDEO button is pressed, that flag is checked to see if the Video Option checked ok at power-up. If the test was not ok, the error message is displayed and the warning bell is sounded. If no error message is displayed, but test 2180 (FLD2) fails either at power-on or during a subsequent SELF TEST, troubleshoot as indicated in Table 6-6 Procedure 7 "Extended Diagnostics" for that failure.

Troubleshooting Procedure:

1. Check A12U830 pin 3 (schematic diagram 1) for two negative strobes about 10.5 μs apart. (Viewing scope Sec/Div at 2 μs, trigger on negative slope of the signal.) If not present, replace U830.

   NOTE

   The $\overline{GPIBSEL}$ signal also selects the Video Option registers. If communication via the GPIB interface is ok, then the select signals to Data Bus Buffer U532 (schematic diagram 20) and the buffer itself are ok. Suspect a problem with Programmable Line Counter U530 (schematic diagram 21).

2. Check U332C pin 8 (schematic diagram 20) for the same negative strobes as at U830 pin 3. If not present, replace U332.

3. Check pins 2, 3, 4, 5, 6, 7, 8, and 9 of Data Bus Buffer U532 for activity (not stuck HI or LO) occurring at the same time as the negative strobe on U332C pin 8. If stuck, troubleshoot the bad bus line.

4. Check that pin 14 of U530 is at +5 V and that pin 1 is ground. If not, troubleshoot the cause.

5. Check that pin 8 of U530 is HI and that activity is occurring on pins 10, 11, 12, 13, 15, 16, and 17. If no activity, troubleshoot the problem.

6. If all inputs to U530 ok, replace U530.

Table 6-7 (cont)

VIDEO TRIGGER PROBLEM	Auto triggering or unstable trigger in VIDEO CPLG:

INITIAL SETUP:

Apply a negative-sync, flat-field, video signal to the CH 2 input. Select the correct protocol (System M or Nonsystem M) for the applied signal using the Extended Functions menus.

Set the following controls:

SLOPE/SYNC	– (negative sync)
VERTICAL MODE	CH 2
TRIGGER MODE	AUTO LEVEL
TRIGGER CPLG	VIDEO
TRIGGER SOURCE	CH 2
SEC/DIV	20 μs
A TRIGGER HO	0 (no HO symbol displayed)
VOLTS/DIV	1 V

Press SET TV and select:

A TV COUPLING	TV LINE
CLAMP	OFF

1. Check the $\overline{\text{TVTG}}$ signal at U524B pin 8. If signal is present and no triggering is occurring, troubleshoot the Trigger Logic Array, A10U370 (schematic diagram 11).
2. If signal is absent, check the ATHO signal line at U424C pin 5 for HI-to-LO and LO-to-HI transitions. If not there, troubleshoot the Holdoff circuit (schematic diagram 13) as indicated in Table 6-6 in "HOLDOFF PROBLEMS".
3. If the ATHO signal is ok, check U424C pin 6 for an inverted ATHO signal; if not present, replace U424.
4. Check that U541B pin 6 has a positive pulse coincident with ATHO transitions. If not, replace U541.
5. Check that U524A pin 5 has a positive pulse coincident with the ATHO transitions. Check that U524A pin 3 is HI. If pin 3 is HI and pin 5 does not follow the ATHO transitions, replace U524.
6. Check pin 8 of U524B for a negative ($\overline{\text{TVTG}}$) pulse coincident with the LO-to-HI ATHO transitions. If not present, check that the TVENA signal on pin 12 is HI and that the HORIZCLK input on pin 11 (see waveform 163) is ok. If those signals are correct, replace U524; if not correct, troubleshoot the source of the problem.
7. Check the test waveforms shown for schematic diagram 21 (waveforms 159 through 168). Troubleshoot the circuitry indicated by an incorrect waveform (see the following troubleshooting procedures).

Table 6-7 (cont)

SIGNAL PROCESSING PROBLEM	See INITIAL SETUP in VIDEO Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to 5 μs and the Volts/Div to 2 V.
	1. Check U610 pin 5 for a horizontal line sync signal having the negative sync tip at about 0.5 V and a back-porch level of +4.5 V. If correct, check pin 6 of U420B for the correct signal (see waveform 162). If not correct there, troubleshoot the Sync Pickoff Comparator (Q504 and Q510) and Pulse Stretcher circuits.
	2. Check that U750 pin 16 (schematic diagram 20) is LO with negative sync selected and HI with positive sync selected. If not, troubleshoot U750.
	3. Is the TVRC signal present at U612 pin 3 (waveform 159)? If not, troubleshoot the source of the TVRC signal (Q140 and U150) and the connecting signal path.
	4. Set the Input Coupling on the scope to GND and check that the dc levels at U612 pins 3 and 13 are about the same. If not, troubleshoot U710B and associated circuitry.
	5. Set the Input Coupling to DC and check that the negative sync tip amplitude at U610 pin 9 is about 50 to 75 mV (from back-porch level to negative tip) with about a −3 V dc offset. If yes, the AGC amplifier and Sync Tip Clamp circuit are ok. Troubleshoot the Fixed Gain Amplifier, the Sync Pickoff Comparator, the Trigger Back-Porch Clamp, and associated circuitry. If the signal is not correct at pin 9 of U610 with the correct TVRC signal applied, troubleshoot the AGC amplifier and Sync Tip Clamp, and associated feedback circuitry.
	6. Set Input Coupling to GND and check that U510 pin 6 is within 1 V of ground level. If not, troubleshoot U510 and associated circuitry.
PHASE-LOCKED LOOP PROBLEM	1. Set the Trigger CPLG to VIDEO, Trigger SOURCE to CH 2, Trigger SLOPE to −(neg-sync), A VIDEO COUPLING to FIELD1—Line count to 10, CH 2 input coupling to DC, SEC/DIV to 200 μs, VIDEO CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect a negative sync composite video signal to the CH 2 input.
	2. Check pin 13 of U314 for narrow positive pulses that coincide with the horizontal sync pulses of the applied video signal. If not present, suspect the Phase Locked Loop circuitry and its input and output signals.
	3. Check Q330, CR324, CR326, CR325, and VR234 for opens or shorts.
	4. Check U308B pin 3 for a LO pulse coincident with the Horizontal Sync of the applied video signal. If not present, check for the presence of the $\overline{\text{COMPSYNC}}$ signal at U310A pin 5 (waveform 169). If $\overline{\text{COMPSYNC}}$ is ok, but the signal at U308B pin 3 is not, troubleshoot U420 and associated circuitry. If both are missing, troubleshoot back through the Video Option input and signal processing circuitry to find the problem.
	5. Check the following signals: 2XH at U314 pin 4, $\overline{\text{2XH}}$ at U308A pin 9, $\overline{\text{HORIZCLK}}$ at U220B pin 12, HCLK at U220B pin 13, DLY'D HCLK at U220A pin 1 (held LO when the PLL is unlocked), VERTSYNC at U310A pin 1. Troubleshoot the cause of any missing signals. (See Figure 3-14 in Section 3 for typical waveforms.)

Table 6-7 (cont)

INCORRECT LINE COUNTING

See INITIAL SETUP in VIDEO Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to 5 μs and the Volts/Div to 2 V.

1. Check that the correct protocol and Counter Restart choices are selected for the applied Video signal. (TV OPT under the EXTENDED FUNCTIONS—SYSTEM choices.)
2. Check that the $\overline{\text{HORIZCLK}}$ signal at U220B pin 12 is stable. If not, troubleshoot that problem.
3. Check that the FIELD signal at U424E pin 13 is stable and correct (waveform 164). If not, troubleshoot that problem. (Is the trigger signal amplitude excessive, causing erratic triggering?)
4. If the FIELD and $\overline{\text{HORIZCLK}}$ signals are ok, suspect a problem with Line Counter U530, NAND-gate U541, or U424.
5. Check that the FLD1 signal at U541 is HI when FLD1 is selected and alternates HI-to-LO when ALT is selected. If not, troubleshoot A12U750 (schematic diagram 20). (This assumes that the FLD2 diagnostic test passed the power-on diagnostics.)
6. Check Line Counter outputs at pin 27 and pin 3 for a LO-to-HI transition during the vertical sync pulse time. (View the composite video on channel 2 of the test scope and use the channel 1 probe to check the signal at pin 27 and pin 3. Trigger the test scope on the channel 1 signal. Use delayed sweep to view the signals if using an analog test scope.)
7. If not correct, replace U530.
8. Check that the clock at pin 8 of U424D is stable and has a LO-to-HI transition. If no transition, replace U424.

TV CLAMP PROBLEM

NOTE

The Video Option must have a composite-sync or composite-video signal source applied for the Channel 2 Display Clamp to function properly. Clamping action is unpredictable if an incorrect signal is applied. The CLAMP circuit remains on, even if VIDEO COUPLING is not selected, and may be used to clamp a Channel 2 display if the selected VIDEO source signal is a composite-sync or composite-video signal.

1. Set the Trigger CPLG to TV, Trigger SOURCE to CH 2, Trigger SLOPE to — (neg-sync), A COUPLING to FIELD1—Line count to 50, CH 2 input coupling to DC, SEC/DIV to 5 μs, CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect the negative sync composite video signal to the CH 2 input in series with a dc offset voltage source. Set the offset level for 0 V offset.
2. Is the display triggered and stable? If not, the CLAMP circuit will not be properly enabled in any case, and some other problem may exist. Check that the collector of Q330 is LO. If not LO, either the PLL (U314) is not locked or Q330 or its associated circuitry is defective; go to PHASE-LOCKED LOOP PROBLEM troubleshooting.
3. If the display is triggered correctly, check that the back-porch level of the displayed video signal is at approximately ground level. If not, run SELF CAL and check again. If there is a large offset present, troubleshoot CH 2 Preamp U320 and U230 (schematic diagram 9).
4. Set the offset voltage for −1.5 V offset, and verify that the back-porch level is offset from ground −1.5 V.
5. Set CLAMP ON. Is the back-porch level clamped to ground level? If so, the VIDEO clamp is functioning.

Table 6-7 (cont)

6. Did the CH 2 signal display change vertical position by any amount when CLAMP was turned on? If not, check that BPCLAMP is HI with CLAMP ON. Troubleshoot A12U750 (schematic diagram 20) if not correct.

7. Check that pin 3 of U410A has a 10 V positive pulse at the beginning of the back porch of the applied video signal (waveform 165). If not, troubleshoot U410A and associated components.

8. Set the test scope BW Limit to 20 MHz and the Volts/Div to 50 mV. Check U520 pin 3 for a CH 2 PO signal that is a replica of the applied video signal. If not present, troubleshoot the CH 2 Preamplifier Pickoff circuitry and the signal path between it and pin 3.

9. Check that pin 6 of U520 is approximately 0 V with the CLAMP OFF and approximately −130 mV with the CLAMP ON. If not switching correctly between CLAMP ON and CLAMP OFF, troubleshoot U410C, Q420, and U520.

10. Switch CH 2 INVERT ON check pin 6 of U520 again as in step 9. If not correct, troubleshoot U514, U410B, U410E and the CH 2 INV signal (should be HI with CH 2 INVERT ON).

11. Check U710D pin 14 for approximately 0 V with CLAMP OFF and approximately −130 mV with CLAMP ON. If not correct, replace U710. Check that the Source of Q710 follows pin 14 of U710D for CLAMP ON and CLAMP OFF. If not, troubleshoot Q710, U710A, and associated components.

FRONT-PANEL SETTINGS FOR INIT PANEL

Table 6-8 lists the front-panel settings which are returned when INIT PANEL is executed from the AutoStep menu (PRGM).

Table 6-8
INIT PANEL States

AUTOSETUP Controls	
Mode	VIEW
RESolution	LO
CURSOR Controls	
CURSOR/DELAY Knob	CURSOR POSITION
CURSOR FUNCTION	All off
VOLTS UNITS	VOLTS
TIME UNITS	SEC
SLOPE UNITS	VOLTS/SEC
CURSOR Mode	Δ
ATTACH CURSORS TO:	CH 1
X-Axis Cursor Position	±3 divisions
Y-Axis Cursor Position	±3 divisions
TIME Cursor Position	±4 divisions
VOLTS Ref Value	1.0 V
TIME Ref Value	1.0 SEC
SLOPE Ref Value	1.0 V/SEC

DELAY Controls	
DELAY by EVENTS	OFF
Δ TIME	OFF
DELAY TIME	40 μs
Δ DELAY Time	0.0
DELAY EVENTS Count	1
DEVICES/SETUP (OUTPUT)	
DEVICES	
HPGL PLOTTER	OFF
THINKJET PRINTER	ON
SETUP	
Print SETTINGS	ON
Print TEXT	ON
Print GRAT	ON
Print WFM	ON
PGSIZE	US

Table 6-8 (cont)

GPIB SETUP (OUTPUT)	
DEBUG	OFF
LONG	ON
LOCK	LLO
PATH	ON
RQS Mask	ON
OPC Mask	ON
CER Mask	ON
EXR Mask	ON
EXW Mask	ON
INR Mask	ON
USER Mask	OFF
PID Mask	OFF
DEVDEP Mask	ON
Data Encoding (ENCDG)	BINARY
Data Target	REF 1
Data Source	CH 1
FASTXMIT	OFF
FASTXMIT	1
CURVE ONLY	OFF
START	256
STOP	512
LEVEL	0
HYSTERESIS	5
DIRECTION	PLUS
SETUP ATTRIBUTE	0
DT	OFF

HORIZONTAL Mode Controls	
MODE	A
A SEC/DIV	1 ms
EXT CLK Expansion Factor	1
EXT CLK	OFF
POSITION Waveform	LIVE
POSITION Reference	REF 1
POSITION set to	Midscreen
POSITION REF mode	INDependent

INTENSITY Controls	
SELECT	DISP
READOUT Intensity	50%
DISP Intensity	40%
GRAT Illum	0%
INTENS Level	80%
VECTORS	ON

MEASURE Controls	
MARK	OFF
DISPLAY	OFF
WINDOW	OFF
METHOD	MIN/MAX
LEVEL (units)	%
LEVEL (settings)	
PROXIMAL	10%/0.4 volts
MESIAL	50%/1.3 volts
MESIAL2	50%/1.3 volts
DISTAL	90%/2.4 volts
TARGET	CH 1

STORAGE Mode Controls	
STORAGE Mode	SAVE
ACQUIRE Mode	NORMAL
REPET	OFF
AVG Number	2
ENVELOPE Number	1
SAVE ON Δ	OFF
REF1 through REF4	OFF

TRIGGER Controls	
A/B TRIG set for	A
A TRIG MODE	AUTO LEVEL
B TRIG MODE	RUNS AFTER
SOURCE (both)	CH 1
COUPLING (both)	DC
SLOPE (both)	+ (plus)
TRIG POSITION	½ (512)
LEVEL (both)	0.0
EXT GAIN (both)	÷ 1
HOLDOFF	Minimum

VERTICAL MODE Controls	
CH 1	ON
VOLTS/DIV (both)	100 mV
VARIABLE (both)	CAL
COUPLING (both)	DC
50 Ω (both)	OFF
INVERT (both)	OFF
POSITION set to	Mid screen
Display Mode	YT
BANDWIDTH	FULL
SMOOTH	OFF

Table 6-8 (cont)

VIDEO OPTION Setup (SET TV)	
Interlaced Coupling	FIELD1
Noninterlaced Coupling	FIELD1
TV SYNC	– (minus)
CLAMP	OFF
Line Count	525
Line Start	PREFLD

WORD RECOGNIZER (SET WORD)	
Word Match	Don't care (all x)
RADIX	HEX
CLOCK	ASYNC